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Self-aligned growth spawns hybrid devices

Enhancing networks with GaN-on-silicon

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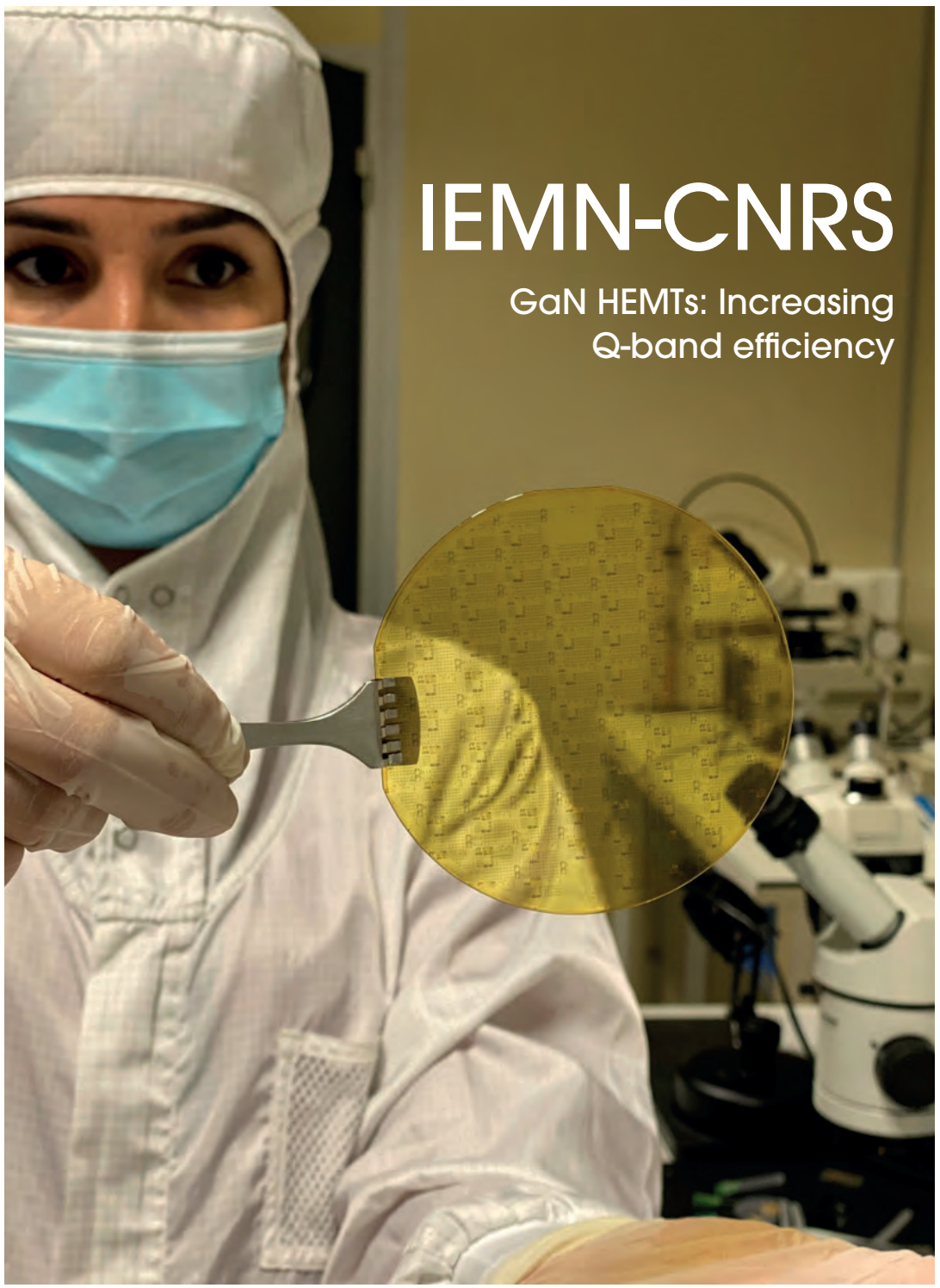
New nanowires yield superior UV LEDs



IEMN-CNRS

GaN HEMTs: Increasing Q-band efficiency

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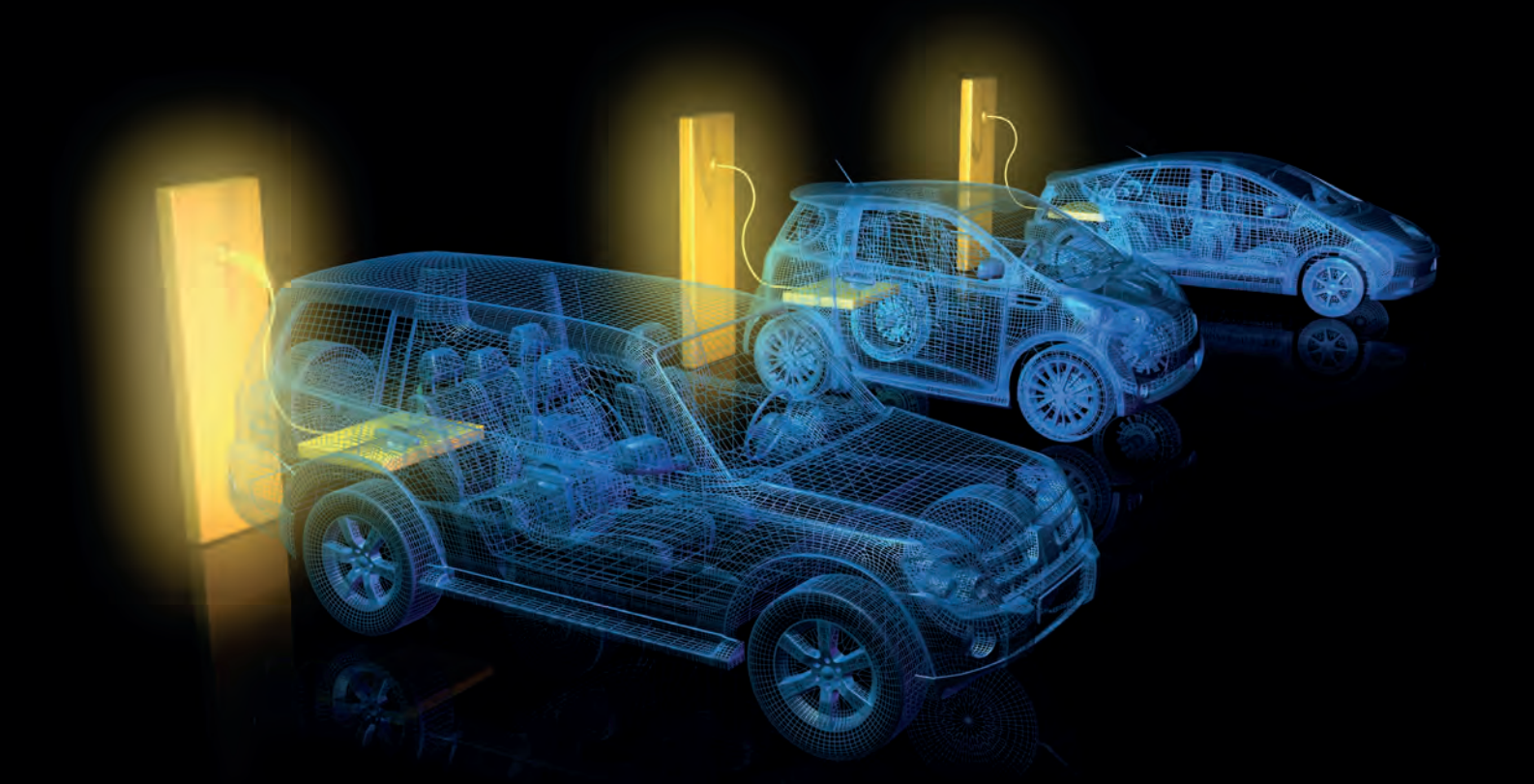

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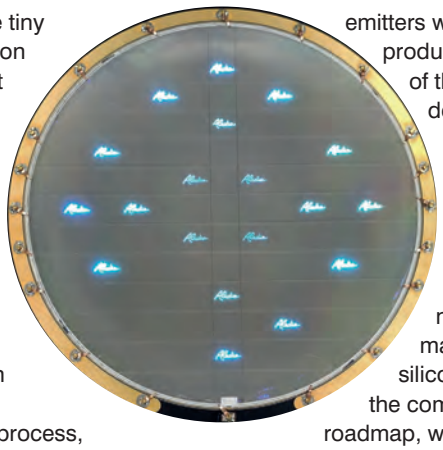
Viewpoint

By Dr Richard Stevenson, Editor

Miniature masterpieces

INTEREST IN microLEDs is rocketing. These tiny emitters, tipped to generate sales of $20 billion within five years, are to be the key ingredient in a new generation of displays that excel in brightness, contrast and reliability.

In this issue, we take a look at this device, considering breakthroughs in red microLED performance, advances in high-volume manufacturing, and how miniaturisation can help in the deep-UV.



There is no consensus on the best approach to making microLED displays. Attracting the most attention is a massive parallel-transfer process, involving picking up arrays of tiny emitters from a growth substrate and putting them down at well-defined locations on a backplane. Ideally, for this approach all microLEDs would be produced from the same class of material. However, right now the best devices on the market for blue and green emitters are based on GaN, while the brightest commercial red emitters come from the GaAs family.

Helping to try and shift to a single-material system, a team from the University of California, Santa Barbara, has fabricated incredibly impressive red microLEDs based on GaN. Key to success is a compliant substrate that quashes light-quenching strain in the active region. On-wafer measurements show that emitters with an active area of only 6 μm by 6 μm can produce an output power density that tops that of the best GaAs-based devices (see p. 50 for details).

In addition to progress in R&D, high-volume manufacturing is essential if the microLED is to net tens of billions of dollars per annum. Addressing that particular goal is French firm Aledia, which has now developed a production process for making nanowire microLEDs from 300 mm silicon. Turn to pages 14 and 15 to hear about the company's revolutionary technology and its roadmap, which includes construction of a 50,000 m^2 manufacturing facility.

In the early years of this millennium, long before interest in microLED displays had surfaced, Asif Khan and his team at the University of South Carolina had started to investigate this technology as a means to combat series resistance and aid current spreading in deep-UV LEDs. Now these engineers are revisiting this architecture, evaluating how pixel size impacts thermal impedance and emission power (see p. 52 for details). Efforts have broken new ground, with claims of the smallest and brightest deep-UV LEDs. So, in future, microLEDs may not only provide us with breath-taking displays – they may also deliver disinfection, by replacing the mercury lamp.

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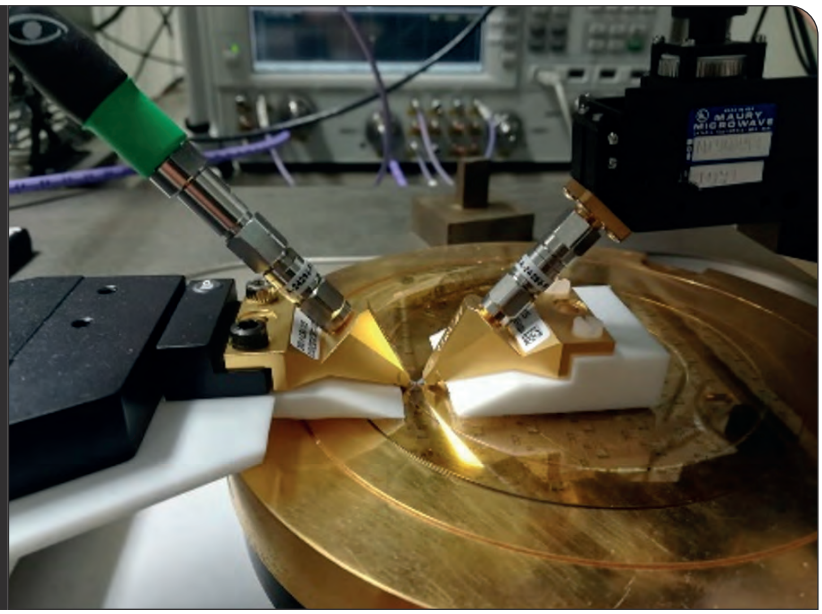

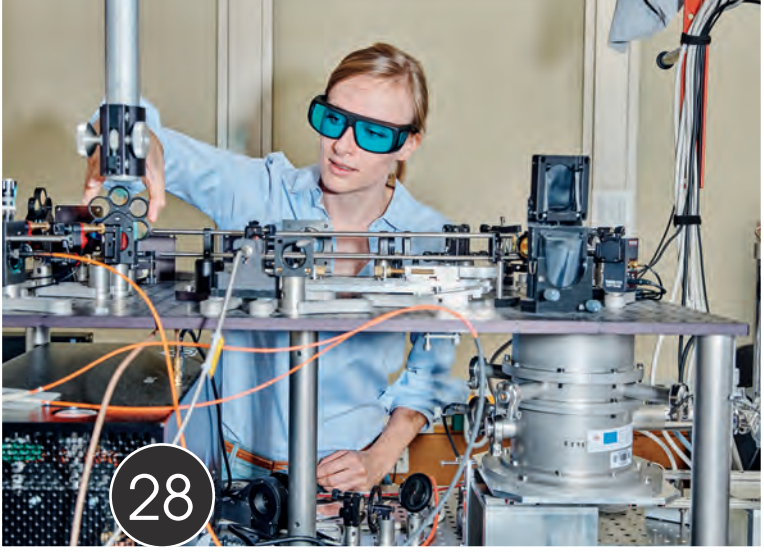

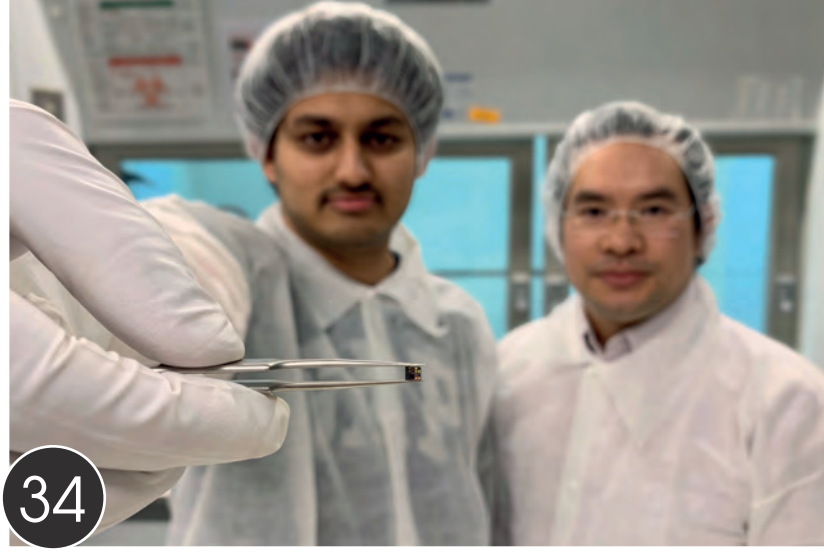

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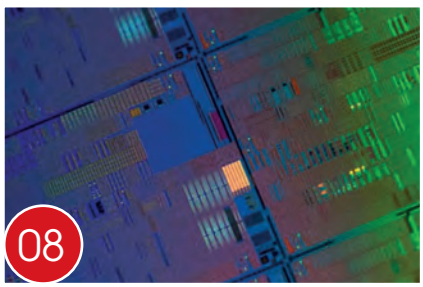

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Osram invests in UV LED specialist Bolb

OSRAM has acquired around 20 percent of California-based UV LED specialist Bolb via its venture capital arm Fluxunit. With its investment in Bolb, Osram says that it is further expanding its technological know-how of disinfection applications with UVC light.

The future cooperation between the two companies in the field of research will accelerate the industrialization of highly efficient and high-performance UVC LEDs.

LED-based disinfection systems require very little space and can be installed directly at the point of use – such as in water taps, washing machines or ventilation systems. Space-saving disinfection solutions make an important contribution to combating the coronavirus. According to Allied Market Research, the market for UV disinfection products is currently worth around one billion euros. This figure is expected to quadruple by 2027. Market researchers also expect the share of UVC LED solutions to grow steadily.

"Osram already has various UVC light solutions for disinfection, including LED and traditional technologies. The strategic investment in Bolb strengthens our know-how in the UVC LED field and gives Osram a leading position in the market for disinfection with non-visible light," explains Ulrich Eisele, head of Fluxunit, Osram's venture capital unit.

Currently, the majority of UVC disinfection applications are based on conventional lighting technologies, usually mercury vapour lamps. Compared with these traditional lamps, UVC LED technology has the potential to consume significantly less energy while still providing the high light output required.

The collaboration between Osram and Bolb promises to overcome this technological hurdle. Thanks to a unique building block for UVC LEDs, Bolb is already succeeding in achieving outstanding efficiency values that are far ahead of other products available on the market.

With Osram's decades of experience in the development and manufacturing of semiconductor-based products, this partnership sets the course for Osram and Bolb to lead the market for UVC LEDs. UVC LEDs promise a variety of benefits for manufacturers of disinfection solutions. These include lower energy consumption, long lifetime and significantly simplified system design, due to the compact size of the light sources.

Kubos Semiconductors shows first commercially compatible cubic GaN LEDs

KUBOS SEMICONDUCTORS, using technology originally spun out of the University of Cambridge, has demonstrated the first commercially compatible LEDs based on the cubic crystal phase of GaN.

David Wallis, Technical Director of Kobos, stated: "This is a culmination of several years of research and development by Kubos and the Cambridge Centre for Gallium Nitride. Using the cubic crystal phase of GaN overcomes the limitations of conventional GaN LEDs allowing us to ultimately deliver significantly higher efficiency green and amber devices."

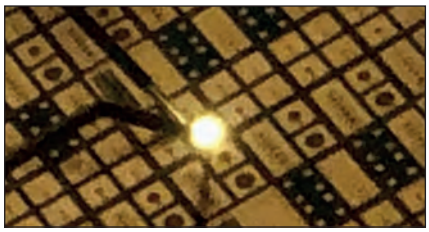
Wallis claims that Kubos' devices underline the material's potential and demonstrate another big step towards achieving full commercialisation.

Having efficient green and amber LEDs will enable the next stage in the development of solid-state lighting (SSL), allowing greater control of the lit environment, further energy savings and carbon impact reduction.

Additionally, by translating the performance benefits of cubic GaN in the lighting sector to smaller devices, this technology could also be a game-changer for microLEDs for full colour displays.

Caroline O'Brien, CEO of Kubos, added: "Previously cubic GaN has been developed as part of small reach activities. The process that Kubos is developing is fully compatible with large scale, volume manufacturing and Kubos holds the unique IP that makes this ground-breaking technological development possible."

"As Kubos opens its next round of funding and broadens customer engagements, these devices further strengthen the arguments for cubic GaN to be used in devices across the visible spectrum and its potential to address both the green gap in LEDs and the current limitations in red microLEDs."



Kubos's technology is claimed to enable the production of commercial high-end, low cost, highly efficient LEDs by fundamentally solving the long-standing green gap problem in SSL. This technology is applicable to a wide range of applications including general lighting, microLED displays, automotive, street lighting and digital signage.

UKRI supports development of GaN HEMT foundry process

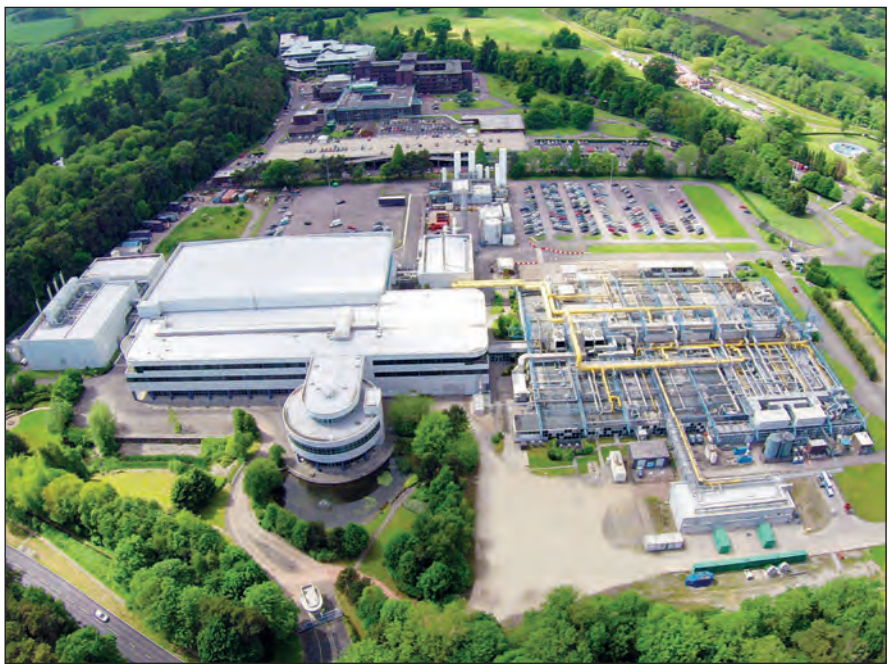
UK RESEARCH AND INNOVATION (UKRI) is supporting the Compound Semiconductor Centre (CSC) and Newport Wafer Fab (NWF) to deliver a foundry grade 650 V GaN-on-silicon HEMT process on a 200 mm wafer platform. The HEMT fabrication process technology will build on 30 years of silicon power device manufacturing heritage at NWF, developed under an automotive (IATF 16949) quality accredited volume manufacturing environment.

The epitaxial solution will leverage IP developed by CSC in partnership with its parent company IQE, on a high-volume Aixtron G5 200 mm manufacturing platform at its Cardiff, UK facility. CSC recently achieved full ISO9001 accreditation of its internal Quality Management System covering development through to volume scale up. The project is supported by UKRI under the *Automotive Transformation Fund: moving the UK automotive sector to zero emissions*.

Sam Evans, NWF's director of external affairs, commented: "This is an exciting step towards NWFs vision of becoming a major manufacturer of compound-on-silicon products. We see the wide bandgap power device market as an excellent area to address in our plans to expand our current manufacturing footprint of 8,000 wafer starts per week to 14,000, and it's a natural opportunity for us to pursue given our heritage in high-power silicon MOSFET, IGBT and GaN device development manufacturing."

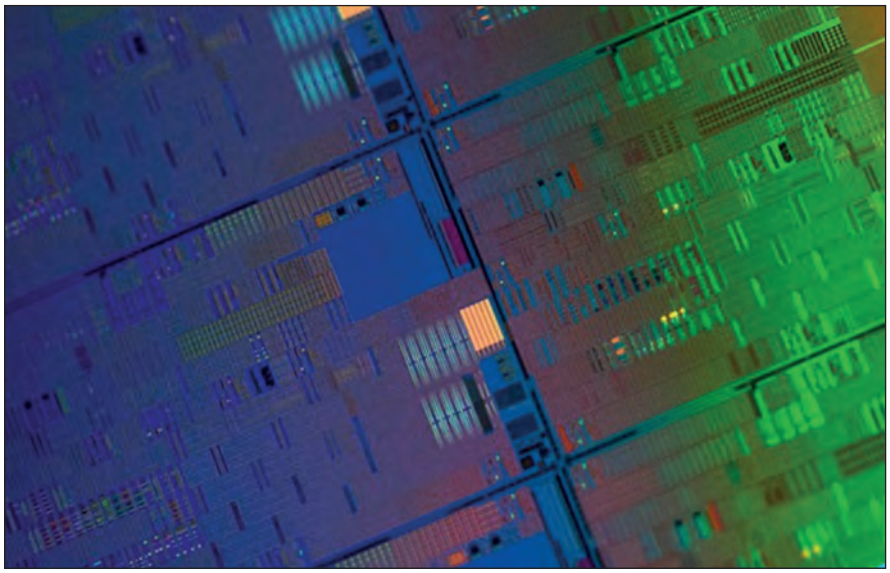
Rob Harper, GaN programme manager at CSC added: "The GaN power market is estimated to be $ 700 million by 2025 with massive future growth opportunity for EV adoption, and we are collaborating with a global power semiconductor blue-chip to help steer the process roadmap. We are initially targeting the EV segment of the market including traction inverters; as the project progresses we hope to role out custom foundry offerings that address additional market segments, including mobile/laptop fast chargers and energy storage inverters."

Wyn Meredith, director of the CSC, commented: "This is an excellent example of two partners in the South Wales semiconductor ecosystem building on their respective technology and manufacturing strengths to offer advanced, next-generation foundry services to the global semiconductor industry."



EC invests €20 million in next-generation electronics

THE EUROPEAN COMMISSION (EC) has announced a €20 million investment in the next generation of electronics and semiconductors. The 2D Experimental Pilot Line (2D-EPL) was announced officially on February 4, 2021, as the first graphene foundry to integrate graphene and layered materials into semiconductor platforms. The new project aims to keep Europe at the forefront of this technological revolution.



Born within the innovative ecosystem pioneered by the EU-funded project, the Graphene Flagship, the 2D-EPL will cover the entire value chain, from tool producers and chemical and material providers to manufacturing lines.

This collaborative project will integrate several Graphene Flagship members to pioneer the fabrication of new prototype electronics, photonic devices and sensors integrating graphene and layered materials.

The 2D-EPL will offer comprehensive prototyping services to companies, research centres and academics, so they can develop and test their innovative technologies based on 2D materials.

“By developing a European pilot line for the processing of graphene and layered materials, we aim to bring these innovative materials from the academic laboratories to the semiconductor production lines, making them compatible with the standards in the industry,” explained Cedric Huyghebaert, technical leader for the 2D-EPL project, and programme manager for exploratory material and module integration at imec, Belgium.

“Moreover, we want to offer early access to experimental pilot line production to the innovative graphene community in Europe. The pilot line will allow them to scale up the production of their innovative devices based on graphene and layered materials.”

Combining graphene and 2D materials with silicon could enhance the potential of electronic technologies, traditionally based on silicon. Nevertheless, integrating both materials at a large scale has been challenging, and up to now advances have progressed at a slow pace, due mostly to a lack of infrastructure.

The 2D-EPL will address this challenge, allowing manufacturers to control the interfaces between silicon and 2D materials on a large scale.

The 2D-EPL will develop the tools, chemistry and materials required for the integration of graphene and layered materials on established semiconductor platforms, which use silicon technologies. The ecosystem and procedures will be validated in state-of-the-art cleanroom environments all around Europe, such as AMO and iHP, Germany; VTT, Finland; and imec, Belgium.

In a later phase, the project will also develop modules to manufacture the basic building blocks for graphene and layered material-based technologies in the fields of optoelectronics, photonics and electronics. These modules will be publicly available for European users through multi-purpose wafers. This strategy will guarantee that these novel technologies are widely available and accessible at a reasonable cost.

The ultimate goal of the 2D-EPL is to build demonstrators and achieve low-volume production of innovative graphene and layered material-based technologies integrated with traditional semiconductors, working closely together with leading Graphene Flagship partners across Europe, including SMEs, industrial companies, research institutions and academic partners.

“For many applications, the wafer-scale integration of graphene and potentially other 2D materials is required for products to appear on the market,” explained Lilei Ye, business developer for Electronics Applications at the Graphene Flagship. “The 2D-EPL will accelerate the manufacture of new prototypes for electronics, photonics and optoelectronics with integrated graphene and layered materials.”

”The 2D-EPL really highlights how the European Commission, through projects like the Graphene Flagship, can make an impact in European research, development and industry,” said Graphene Flagship Director Jari Kinaret. “We identified a challenge – upscaling the production of graphene electronics – and the European Commission heard us, finding funding to address this challenge.”

A large number of partners participating in the new adventure, the 2D-EPL, are also active members of the Graphene Flagship, one of the largest research initiatives ever funded by the European Commission.

The 2D-EPL will work closely with the Graphene Flagship to understand the fundamentals of graphene and layered materials and establish a plan to bring these materials to market.

II-VI unveils VCSEL arrays for next gen 3D sensing

II-VI HAS announced its double-junction VCSEL arrays, the first of its multi-junction VCSEL array platforms for next-generation world-facing 3D sensing applications.

The growing adoption of 3D sensing in several markets, including in consumer electronics, automotive, and industrial, is driving the demand for depth sensors with a longer and wider range, lower power consumption, smaller size, and lower cost.

II-VI's new VCSEL arrays are based on a double-junction technology that doubles the power output per VCSEL emitter and improves the power conversion efficiency to 56 percent, compared with 46 percent in existing single-junction technology. This can be leveraged for a number of differentiating benefits, including higher output power to sense farther and wider, reduced battery power consumption, and smaller size to achieve lower cost and to enable more inconspicuous designs.

"We have developed over the years strong partnerships with our customers, closely collaborating on the development of long-term technology and product roadmaps aimed at providing breakthrough solutions and continuously elevating user experience in 3D sensing," said Julie Eng, SVP, Optoelectronic & RF Devices Business Unit.

"A few years ago, we successfully scaled our vertically integrated GaAs optoelectronics technology platform from 3-inch to 6-inch, which enabled us to shorten our development cycles and introduce new products to meet aggressive market windows. We are now once again evolving the platform, this time with a leap to double-junction technology that we believe will unlock exciting new use cases, such as farther depth of sensing in world-facing applications and seamless integration into consumer products for AR and VR applications."

II-VI's double-junction VCSEL arrays emit at 940 nm, and their steep slope efficiencies enable very short pulses of very high peak powers.

The VCSEL arrays are designed for low-cost non-hermetic packaging and, like the single-junction arrays, can be reliably and cost-effectively scaled in total power by increasing the number of emitters per chip. They can also be produced in high volume on II-VI's vertically integrated 6-inch platform.

II-VI's broad portfolio of products for 3D sensing includes diffractive optical elements (DOEs) and thin-film filters that are produced at wafer-scale for high-volume applications. DOE flat lenses and lenslet arrays collimate, focus, or transform beams from VCSEL arrays. DOE diffusers homogenize the output of VCSEL arrays and produce a uniform field of illumination. DOE splitters separate an input beam into multiple output beams. Filters are used to improve the signal-to-noise ratio of the image sensor array. II-VI VCSEL arrays are available as chips or integrated with DOEs in surface-mount technology packages.

ON Semi announces new 650 V SiC MOSFETs

ON SEMICONDUCTOR has announced a new range of SiC MOSFET devices for demanding applications where power density, efficiency and reliability are key considerations. By replacing existing silicon switching technologies with the new SiC devices, designers will achieve significantly better performance in applications such as electric vehicles, on-board chargers, solar inverters, server power supply units, telecoms and uninterruptible power supplies.

ON Semiconductor's new automotive AECQ101 and industrial-grade qualified 650 V SiC MOSFETs provide superior switching performance and improved thermals when compared to silicon.

This results in improved efficiency at the system level, enhanced power density, reduced electromagnetic interference and reduced system size and weight.

The new generation of SiC MOSFETs employ a novel active cell design combined with advanced thin wafer technology enabling best in class figure of merit R_{sp} (the product of R_{dson} and area) for 650 V breakdown voltage.

The NVBG015N065SC1, NTBG015N065SC1, NVH4L015N065SC1 and NTH4L015N065SC1 have the lowest R_{dson} (12 mΩ) in the market in D2PAK7L and To247 packages.

This technology is also optimised around energy loss figure-of-merits, optimizing performance in automotive and industrial applications. An internal gate resistor allows more flexibility to designers eliminating the need to slow down devices artificially with external gate resistors. Higher surge, avalanche capability and short-circuit robustness all contribute to enhanced ruggedness that delivers higher reliability and longer device lifetimes.

Commenting on the new releases, Asif Jakwani, senior vice president of the Advanced Power Division at ON Semiconductor said: "In modern power applications such as on-board chargers for EV and other applications including

renewable energy, enterprise computing and telecom, efficiency, reliability and power density are constant challenges for designers.

"These new SiC MOSFETs significantly improve performance over the equivalent silicon switching technologies, allowing engineers to meet these challenging design goals. The enhanced performance delivers lower losses that enhance efficiency and reduce thermal management needs as well as reducing electromagnetic interference. The end result of using these new SiC MOSFETs is a smaller, lighter, more efficient and more reliable power solution."

II-VI Unveils VCSEL flood illuminator modules

II-VI, a provider of semiconductor lasers and micro-optics for consumer electronics, has announced VCSEL flood illuminator modules for driver and occupancy monitoring systems in vehicles.

US and European transportation safety regulators are increasingly recommending or requiring driver and occupancy monitoring systems in vehicles, spurring the demand for next-generation 2D and 3D infrared cameras designed with higher-performance infrared illuminators.

II-VI's new VCSEL flood illuminator modules emit higher optical power and with a narrower spectral width than infrared LEDs currently used in existing driver monitoring systems, enabling substantial improvements in system performance.

The infrared light emitted from II-VI˙s flood illuminator modules can be modulated to frequencies greater than 100 MHz, making them ideal for 3D time-of-flight cameras for driver and occupancy monitoring systems.

"Our new VCSEL flood illumination modules integrate VCSEL chips, photodiodes, and diffuser optics, achieving a greater level of vertical integration and value for our customers", said Julie Eng, SVP, Optoelectronic & RF Devices Business Unit.

"We leveraged our in-house 6-inch GaAs technology platform to successfully scale production of our VCSEL arrays for consumer electronics, and we look forward to ramping production of flood illumination modules for in-cabin sensing in automotive as the demand grows."

II-VI˙s VCSELs achieve high power-conversion efficiency and are available with up to 2.5 W or 5 W of continuous power output. The flood illuminator

modules are available in surface-mount packages integrated with diffuser optics with either a narrow (60° x 45°) or wide (110° x 85°) field of view. The modules are expected to be AEC-Q102 certified for automotive applications in the second quarter of calendar 2021.

II-VI's portfolio of products for sensing includes infrared VCSEL chips with one or up to hundreds of elements. II-VI also offers thin-film filters and diffractive optical elements, including lenses, micro-lens arrays, diffusers, and splitters, that are produced at wafer-scale for high-volume applications.

Cambridge GaN devices secures £6.8 million funding

CAMBRIDGE GaN DEVICES (CGD), a fabless Cambridge University spin-off, has secured £6.8 million of funding in a Series A round.

The funding round was co-led by IQ Capital, Parkwalk Advisors, and BGF. It also included investment from Foresight Williams, Cambridge Enterprise, Martlet Capital, Cambridge Angels, and Cambridge Capital Group.

CGD will use the funding to double staff and expand its GaN product portfolio following decades of research in power devices.

Founded by Giorgia Longobardi and Florin Udrea in 2016, CGD designs, develops, and commercialises GaN transistors and ICs enabling a radical step change in energy efficiency and compactness. CGD is suitable for high-volume production.

The company is developing a range of GaN transistors that are customised for key applications in market segments such as consumer and industrial switch-mode power supply (SMPS), lighting, data centres, and automotive HEV/EV.

CGD is currently leading GaNext; a $10 million European-funded project with 13 industrial and academic partners that will develop GaN-based modules for low and high-power applications.

Longobardi, CEO, and founder of CGD commented: "This latest round of investment is a great recognition of our success to date, with new and existing investors confirming the strength of our technology. Since 2016, CGD has grown significantly and we are thrilled to be in a position to deliver several products to market, following decades of industry-leading research in the reliability of power devices.

Investment will allow CGD to supplement its team with additional experts and expand markets globally, creating more sustainable electronics worldwide.

Eric Stodel, CEO at Neways, partner in the GaNext project, commented: "Our close collaboration with CGD has been an incredibly rewarding win-win experience. It enables us to develop an extremely compact solar inverter based on GaN technology."

Stodel added: "The team's enthusiasm is inspiring and contagious, and the shared expertise within our companies has been instrumental in making our combined project a great success with much more future potential".

Ed Stacey, the managing partner at IQ Capital, commented: "We are proud to support the CGD team as they build on their core technology, from a strong base of academic research and IP, to create the world's best GaN power devices for a wide range of applications. This highly experienced team has incredible potential to disrupt the electronics industry with new devices that will unlock commercial and environmental gains for suppliers and customers."

John Pearson, investment director at Parkwalk Advisors, commented: "Parkwalk are delighted to have completed this investment into CGD, with their ambitious and experienced team, we are excited to continue supporting them on their journey to commercialise their innovative and highly disruptive technology."

Tim Rea, the investor at BGF, commented: "Cleantech and sustainable investments are at the heart of BGF's growth strategy for 2021 and beyond. CGD's technology has the power to make a significant impact on power consumption. Its founders are second-to-none and we look forward to working with them, and a cohort of brilliant co-investors, to bring this product to market."

Nick Mettyear, investment manager at Foresight Williams, commented: "The team is designing market-leading products with a huge range of practical uses. Their devices will ultimately improve performance, reduce cost and lead to reduced emissions. It is a perfect fit with Foresight Williams, and we are excited to support the team."

IQE reaches milestone for templates for RF filters

WAFER PRODUCTS firm IQE has announce the achievement of the next milestone for IQepiMo template technology for high performance AlN based bulk acoustic wave (BAW) RF Filters. Customer device data demonstrates that filters fabricated using IQE templates show improved performance when compared with incumbent technology.

Following IQE's announcement in November 2020, the company has sampled its IQepiMo product to multiple customers and partners. Recent data indicates that IQepiMo enables customers to achieve improved electromechanical coupling (as measured by k^2), a key measure of filter performance, compared with conventional technology.

Initial data indicates k^2 increases of as much as 40 percent at a frequency of 6 GHz. This frequency is at the top end of the ranges used in current 5G applications, and within the industry it is proving difficult to achieve high levels of performance using conventional BAW filter technology at these higher frequencies.

The data also confirms that the superior material quality achievable using IQepiMo is linked to significant improvement in electromechanical device performance, especially at these higher frequencies.

IQE and its partners remain engaged in multiple formal programmes to further refine this technology for high end BAW filters.

In particular, it is expected that IQE's templates will provide significant benefit for high scandium-content ScAlN BAW designs that are being targeted for high performance filters at the higher 5G frequencies.

As scandium content increases in BAW filters, maintaining high acoustic material quality and thereby performance becomes ever more challenging. IQepiMo offers customers a route to overcoming these inherent challenges whilst still using their current infrastructure and processes.

Built on its cREO technology platform, IQepiMo templates are available in diameters of up to 200 mm. Rodney Pelzel, Chief Technology Officer of IQE, commented: "I am pleased to announce that we have confirmed that the superior material characteristics of IQepiMo templates translate to improvement in RF filter device performance."

"This is a key milestone. IQepiMo template technology provides customers a 'drop in' improvement that enables current infrastructure and processes to deliver the demanding performance required for 5G applications, especially at higher frequencies."

Oxford Instruments Plasma Tech is on the move

Oxford Instruments Plasma Technology, a provider of wafer processing solutions, has announced plans to move to a state-of-the-art manufacturing facility on the outskirts of Bristol, UK. The relocation is driven by the growing demand from customers.

Managing director of Plasma Technology, Matt Kelly, comments: "The continued and accelerating demand for our production and research solutions has meant it's time to create a new facility. Our new site will be a leading-edge laboratory, manufacturing and office environment for our colleagues, customers, and collaboration partners; an inspiring environment that supports team working, innovation, training and provides greater flexibility."

"Our customers will have even more opportunity to see our solutions and train at our facility. Our building will also be an excellent base to welcome community groups, such as schools and universities promoting STEM subjects."

Kelly continues: "The new premises is just twenty minutes away from our current site and is a purpose-built facility in Bristol. We took the decision to keep our manufacturing and R&D facilities in the Bristol area, for several reasons. Our employees are of utmost importance to us and limited disruption to their current work/home life balance was key. We are also passionate about our involvement in and support of the local economy and want to maintain our contribution here. As we grow further, we will continue to provide additional employment opportunities in the Bristol/West-Country tech cluster".

The new facility will include ISO 5 & 6 class application laboratories spanning 1,000m^2 equipped with a complete suite of state-of-the-art wafer processing solutions and advanced characterisation/metrology technologies; many of these being supplied by Oxford Instruments businesses.

This will not only enable development of next generation processes for all our customers but also allow continuous improvement, and intense reliability testing of our high-volume manufacturing application processes, combining silicon semiconductor standards with compound semiconductor solutions.

The design of the new site incorporates a range of energy-saving technologies to reduce environmental impact, with the goal to eliminate the use of fossil fuels. This includes the option to generate significant amounts of energy from photovoltaic panels, reusing heat from the building's cooling and heating systems, and harvesting rainwater.

Aledia closes in on microLED displays market

With nanowire chips demonstrated on 300 mm silicon wafers, CEA-Leti spin-out, Aledia, plans to deliver its first products next year. Rebecca Pool talks to chief executive, Giorgio Anania, to find out more.

LATE LAST YEAR, France-based microLED display start-up Aledia claimed a world first by manufacturing its nanowire chips on 300 mm wafers at its CEA-Leti pilot lines. In the last eight years, the company has been carrying out research and development on 200 mm wafers, but having demonstrated the technology on the larger wafer size signals clear ambitions for volume manufacture and market entry.

As Giorgia Anania, Aledia chairman, chief executive and co-founder, tells *Compound Semiconductor*: "This is all about cost – we've been doing R&D on 200 mm wafer sizes as it's cheaper but, for us, the transition to larger wafer sizes is easy."

"We'll release our first products in 2022 on 200 mm wafers, and as soon as we get into volume production the following year, we'll move to 300 mm wafers," he adds.

Aledia's announcement comes at a time when all eyes are on microLEDs. Industry analysts have forecast gargantuan global microLED market growth, in the region of 90 percent CAGR to nearly $20 billion by 2026, as consumers demand brighter and more power-efficient display panels for smart devices and augmented/virtual reality headsets.

These mighty figures are attracting more and more businesses to the market. Key players include industry heavyweights such as Apple, Samsung, Sony, Oculus and LG Display and smaller companies and start-ups including Glo, Plessey, Play Nitride, and of course Aledia.

However, what sets the CEA-Leti spin-out apart is its technology. While most microLED developers have focused on fabricating 2D planar GaN layers on 100 mm and 150 mm sapphire substrates, Aledia has been growing GaN nanowires directly onto large-size silicon wafers. This makes technology and business sense.

For starters, growing vertical nanowires onto silicon prevents the accumulation of wafer stresses that takes place when GaN and InGaN layers are deposited on silicon or sapphire. As Anania highlights: "We don't need buffer layers and we don't have wafer bow – this allows us to transition to any wafer size."

What's more, Aledia will eventually be able to realise the economies of scale that only silicon foundries can bring. Anania is excited.

Highlighting how the entire display market is forecast to turn around $120 billion every year, he intends for his company to target many market segments. These include TVs, laptops and tablets, as well as smartphones, smartwatches and virtual/augmented reality displays. And these segments are largely driven by existing investors.

For example, Intel Capital, with its interest in laptops, tablets and mid-sized displays, has already ploughed millions of dollars into Aledia. At the same time, the company also has several collaborations with unnamed smartphone and augmented-reality players. As Anania points out: "This validates our technology and shows it has enormous potential for the future."

But what about the many issues that have thwarted microLED display development? From word go, display manufacturers have struggled with the mass transfer of microLEDs onto a display backplane.

However, according to Anania, Aledia is developing a parallel method to quickly and effectively transfer millions of nanowires from the wafer, directly onto the display backplane. As part of this, the company has also been working with chip-transfer equipment manufacturers to optimise transfer processes for Aledia wafers.

And while the efficiency of conventional planar microLEDs is known to swiftly drop with pixel size, Anania highlights how the efficiency of his company's nanowires remains unchanged at smaller chip sizes. Indeed, he asserts that nanowire efficiency actually

exceeds that of planar microLEDs at sub-pixel sizes of less than 10 μm, which is critical for displays in smartphones, tablets and augmented-reality devices.

"Most of the [small to mid-size] microLED display market needs 3 to 4 micron sub-pixel sizes to make money and sell at a cost that is lower than OLED displays," he says. "So our nanowires are particularly suited to the vast number of consumer applications that we are targeting."

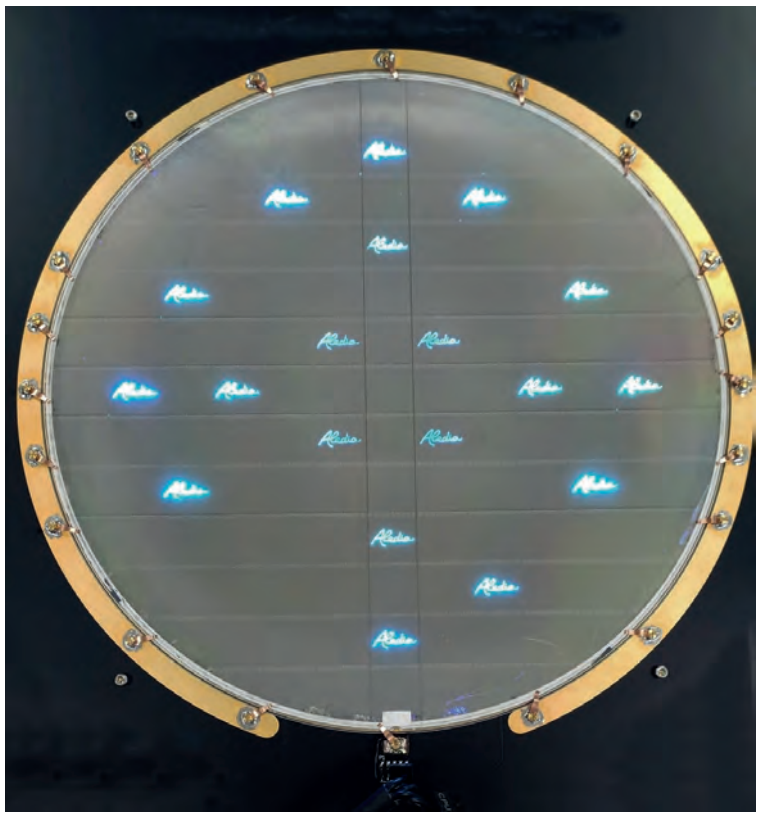
Right now Aledia is developing three nanowire platforms with increasing complexity. Its initial technology comprises blue and colour-converted nanowires and is scheduled for mass production come the second half of 2022. Meanwhile the final platform, which Anania describes as 'revolutionary', will comprise red, blue and green nanowires. Volume production is scheduled to start during 2024, and once ready, this platform will replace the preceding platforms.

The Aledia chief executive won't be drawn on what the company's first products will be. As he puts it: "I think we've been very clear that our high-volume products will fall into the laptop segment of this market, given our collaboration with Intel."

In the meantime, the company is very much focused on building up its manufacturing capacity. As Anania emphasises, during display manufacture Aledia only carries out the necessary nanowire growth and epitaxy, with wafer and chip processing, CMOS integration and back-end testing all taking place in silicon foundries. The company has already revealed a key partner here to be Israel-based Tower Semiconductor.

Aledia began to scale operations in late 2019, re-locating from its original Grenoble-based R&D facility at CEA-Leti to larger headquarters, and research and development facilities, still in Grenoble. And following its latest €80 million financing round, the company is building a high volume, 50,000 m^2 3D microLED manufacturing facility in Grenoble – estimated to cost around €40 million – that is scheduled for completion by the second half of 2022.

"We'll be able to use our existing research and development lab for sales before this, but come the middle of 2023 we're going bigger and will need this facility to be ready for this ," says Anania. Equipment will be brought online for high volumes in 2023.



Aledia's nanowire chips on a 300 mm silicon wafer.

"Unlike companies, such as, say Plessey, we've spent relatively little on manufacturing and equipment in the past, relying on the national lab to do most of our processing," adds Anania.

"But now we're getting close to market so have been accelerating R&D, extending collaborations and buying equipment."

Indeed, Aledia recently purchased a Veeco Propel 300 mm MOCVD system for its epitaxy. And with plans to invest a total of €200 million in equipment – including the latest expenditures – over the next five years, and grow the company to approximately 500 employees, exciting times are ahead.

"Because we're on silicon, we're currently the only company that can take advantage of the cost advantages of manufacturing on 300 mm wafer as well as sophisticated electronics integration," highlights Anania."This will allow us to compete aggressively and be first to market with different types of displays."

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Making more efficient, more reliable millimetre-wave HEMTs

Miniaturized HEMTs equipped with ultra-thin barriers and high-quality passivation enable record-breaking efficiencies in the Q-band

BY KATHIA HARROUCHE, RIAD KABOUCHE AND FARID MEDJDOUB FROM IEMN

FOR RF SYSTEMS, a great deal is gained by going to higher frequencies. To draw on this, during the coming years much effort will be devoted to rolling out next-generation 5G networks, satellite communications and radar systems operating at millimetre-wave frequencies. Moving to this domain satisfies the demand for higher bandwidth, while facilitating higher data transmission rates.

MMICs are now capable of operating at millimetre-wave frequencies, thanks to recent, ongoing progress in device fabrication and processing. When made from silicon, this delivers a few watts below the K_a-band but struggles to produce sufficient power at higher frequencies. Overcoming this weakness is the GaN-based HEMT, a device delivering a strong performance from a small size, thanks to its great material properties that include a wide bandgap, a high electron mobility and high saturated-electron velocity. Armed with all these attributes, GaN-based RF power devices have positioned themselves as ideal building blocks for making MMICs, as they enable a hike in the output power of compact solid-state power amplifiers, so that they can serve more applications.

When deployed in solid-state power amplifiers, a critical parameter for the GaN HEMTs is its power-added efficiency (PAE) – this directly affects its power dissipation. One of the key goals facing developers of GaN HEMTs is to maximise PAE, so that the device can deliver a high output power density (P_{OUT}) in the millimetre-wave range.

In addition to delivering high performance in this domain, GaN-based MMICs must combine robustness with reliability if they are to enjoy success in high-volume applications. Much more work is needed on this front, given that there are very few published reports related to millimetre-wave GaN device reliability. Efforts will need to be directed at scaled material and devices, as this will enable demonstration of high stability, reproducibility and uniformity.

Ultrathin barriers

The tried-and-tested pathway for enhancing the RF performance of semiconductor devices is to scale down transistor dimensions. For GaN HEMTs, this must go hand-in-hand with optimisation of the epilayer stack, especially the top barrier layer. Emerging ultrathin barrier heterostructures, such as AlN/GaN, are a promising architecture for the millimetre-wave range, because they offer the possibility to highly scale the epitaxial structure while retaining the benefits associated with high polarization, such as a high current density.

By adopting this approach, our team from the Institute of Electronics, Microelectronics and Nanotechnology in Villeneuve-d'Ascq, France, has broken the record for PAE at 40 GHz. Crucial to our success has been our collaboration with Soitec-Belgium, the division created through the acquisition of EpiGaN. This partner of

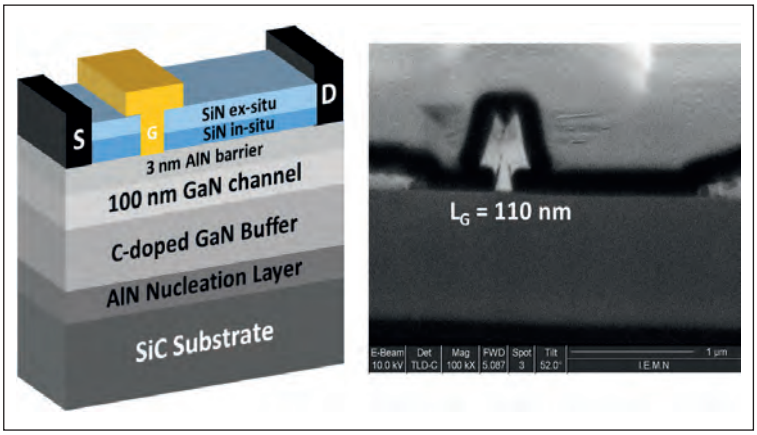


Figure 1: Schematic cross section of an AlN/GaN HEMT (left) and a focused ion-beam view of a 110 nm T-gate (right)

ours, an expert in MOCVD of III-Ns, has provided us with high-quality AlN/GaN heterostructures.

We have fabricated our AlN/GaN HEMTs from epiwafers that feature a SiC substrate and a 3 nm-thick AlN barrier. These devices have a 110 nm T-shaped gate and are capped with a dual purpose 10 nm-thick SiN layer that is grown *in-situ*: it provides early passivation, while reducing trapping effects (see Figure 1 for a cross-sectional diagram of our transistor (a), and a focused ion beam view of the gate (b)).

Despite the use of an extremely thin barrier, our structure has a sheet carrier density within the channel that exceeds 2×10^{13} cm^{-2}, and a mobility of almost 1000 cm^2 V^{-1} s^{-1}. The ultrathin barrier is a tremendous asset, enabling a highly favourable aspect ratio for the gate length to gate-to-channel distance. Thanks to this, our HEMTs offer optimum operation while sporting sub-100 nm gate lengths, a set of

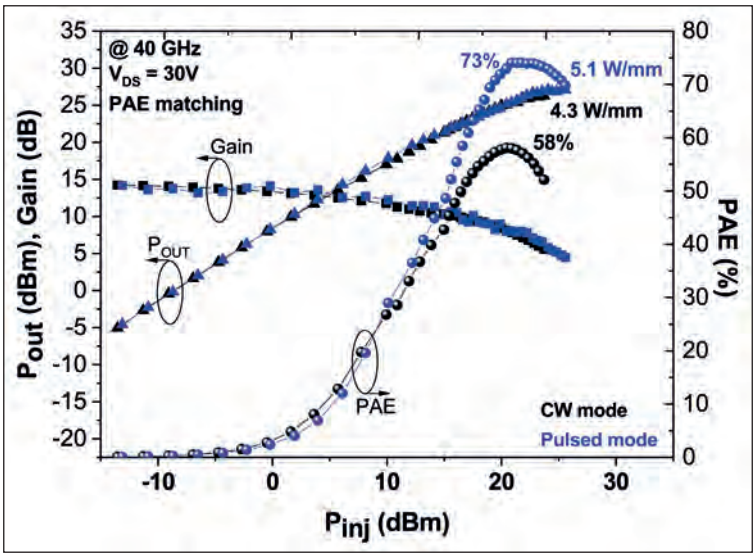
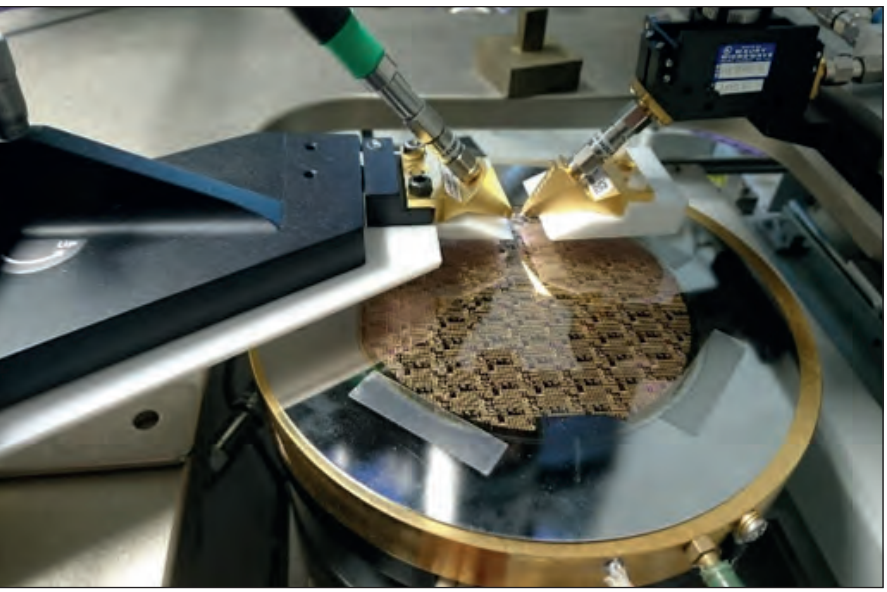


Figure 2. CW and pulsed power performances at 40 GHz of a 3 nm AlN/GaN HEMT 2×50 μm with L_G = 110 nm and L_{GD} = 0.6 μm at V_{DS} = 30 V.



Active load pull measurements at 40 GHz.

characteristics that enable an increase in gain and improved RF performance.

Note that the traditional approach for increasing the aspect ratio is to apply the so-called gate-recess. This brings the gate closer to the channel regardless of barrier thickness, often at the expense of irreversible damage to the crystalline material that leads to serious reliability issues.

A significant threat from downscaling is that it hampers device robustness, a crucial concern for all applications. For ultrashort transistors operating at high drain voltages – they are typically more than 15 V – there is a need for high device reliability and low trapping effects. To excel on both fronts, there need to be high quality material and processing. Both goals can be accomplished by reducing defect density and enhancing surface robustness through the inclusion of an *in-situ* SiN cap layer.

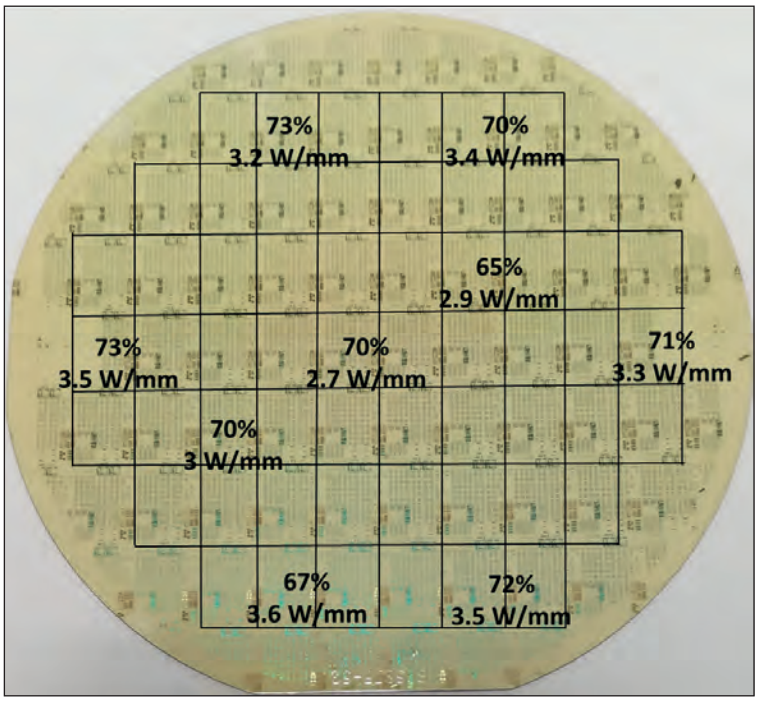


Figure 3. Manuel mapping of 40 GHz pulsed large signal performances at a V_{DS} of 20 V of the 3 nm AlN/GaN wafer with L_G = 110 nm and L_{GD} = 0.6 μm (PAE matching).

Q-band efficiency records

To increase the efficiency of millimetre-wave GaN HEMTs that operate at a high output power density while maintaining strong device robustness, there needs to be an increase in surface stability under a high electric field. We accomplish this by combining optimised processing with the incorporation of an *in-situ* SiN cap layer. Our approach to realising this has been continuously refined over many years, with improvements including reductions in gate resistance and parasitic capacitances. We select a gate-to-drain distance of 0.6 μm, which provides the ultimate trade-off between RF performance and breakdown voltage. Large signal characterization of our HEMTs reveals outstanding power performances at 40 GHz.

Operating in pulsed mode, our devices reproducibly deliver an unprecedented peak PAE of 73 percent with a saturated P_{OUT} above 5 W/mm. For CW operation, this figure falls to 60 percent and 4.3 W/mm, due to residual trapping effects. A key factor in the record-breaking performance of these 2×50 μm transistors is the untypically high drain bias in this frequency band – it can reach 30 V.

Our 4-inch wafers have excellent yield and uniformity, according to manual mapping measurements made on a significant proportion of our HEMTs. Measurements at 40 GHz on 2×50 μm transistors with a 110 nm gate length and a gate-to-drain distance of 0.6 μm show that for a drain-source voltage of 20 V, PAE is typically 70 percent and P_{OUT} 25 dBm. This is a power performance combination that sets a new benchmark in the Q-band.

Increasing the RF performance of the GaN HEMT increases its commercial appeal, but if it is to enjoy market success, it also requires proven reliability. This is the biggest challenge for GaN HEMTs with gate lengths below 150 nm, because compared with qualified GaN technologies, they have a significantly higher electric field peak, and consequently, a high junction temperature under high drain bias.

To gain insight into the robustness of our technology, we have undertaken short-term on-wafer RF stress monitoring. Using a drain-source voltage of 20 V and large signal conditions at 40 GHz, we have recorded the PAE and P_{OUT} for 24 hours, using steps of 4 hours and six different temperatures. Results show that the RF performance remains stable up to a base-plate temperature of 140°C, with no degradation in drain leakage current after the entire

stress test (see Figure 4). As is to be expected for any RF semiconductor technology, the increase in temperature results in a reduction in electron mobility, leading to lower gain and PAE. Note that the initial PAE recovers after the test.

We attribute increased robustness to the higher structural quality of the ultrathin barrier layer and/or the *in-situ* SiN cap layer interface. This has led to an increase in the safe operating area under harsh conditions.

W-band promise

There is growing interest in the W-band, which offers shorter wavelengths and wide frequency bands. Within the W-band, used to conquer new fields of science and industry, is an atmospheric transparency window at 94 GHz that allows for imaging millimetre-wave radar. The 94 GHz frequency also has the potential to be employed for a number of applications associated with defence, astronomy and security.

Our latest generation of devices is not designed to operate in the W-band. For those frequencies, gate lengths need to be below 100 nm. However, to verify the potential of our HEMTs for higher frequency operation, we have undertaken CW large signal characterisation at 94 GHz. Operating at a drain-source voltage of 20 V, our transistors with a 110 nm gate length delivered a CW P_{OUT} as high as 4 W/mm, and an associated PAE of 14.3 percent, limited by power gain (see Figure 5). Moving to shorter gate lengths is sure to lead to a significantly higher PAE.

The results obtained at various frequencies demonstrate a very promising pathway to realising efficient, robust GaN HEMTs all the way to 100 GHz. However, while we are encouraged by a PAE above 70 percent in the Q-band, and the accompanying short-term reliability at high temperatures, we acknowledge that there is still much work to do. There is a need to demonstrate state-of-the-art performance at the MMIC level, alongside long-term reliability – that must include monitoring that lasts for several-thousand hours. Another direction worthy of attention is to investigate refining the heterostructure to further decrease trapping effects. Succeed in this endeavour, and the door could open to an even larger number of applications involving GaN HEMTs operating in the millimetre-wave.

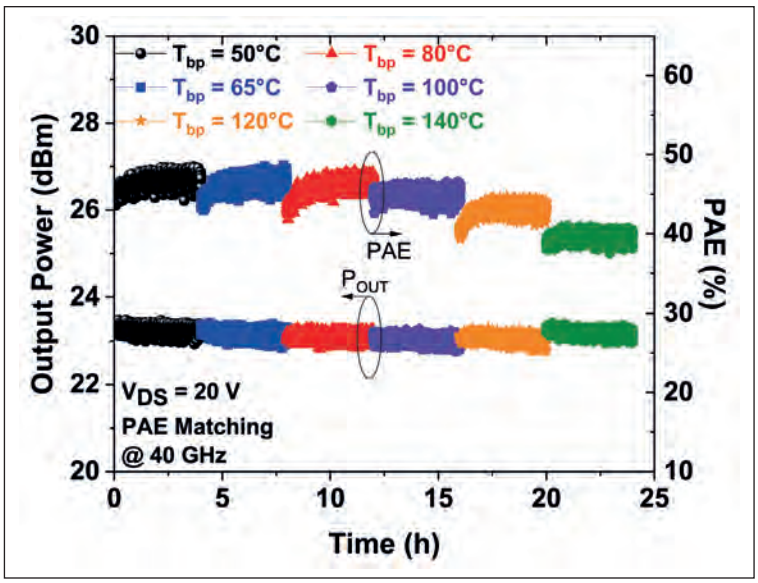


Figure 4. CW output power and PAE monitoring for 24 hours at several base plate temperatures up to 140°C with V_{DS} = 20 V (PAE matching) of a 3 nm AlN barrier HEMT.

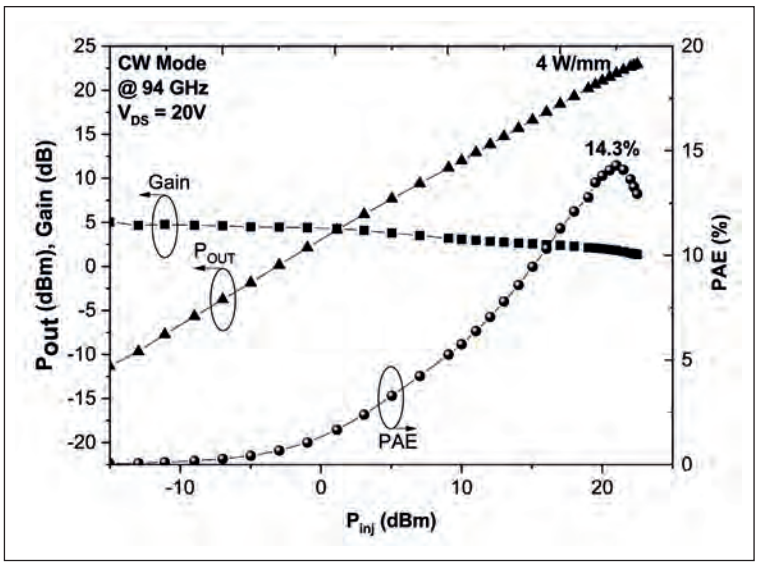


Figure 5. CW power performances at 94 GHz of an AlN/GaN HEMT 2×25 μm with L_G = 110 nm for L_{GD} = 0.6 μm at V_{DS} = 20 V.

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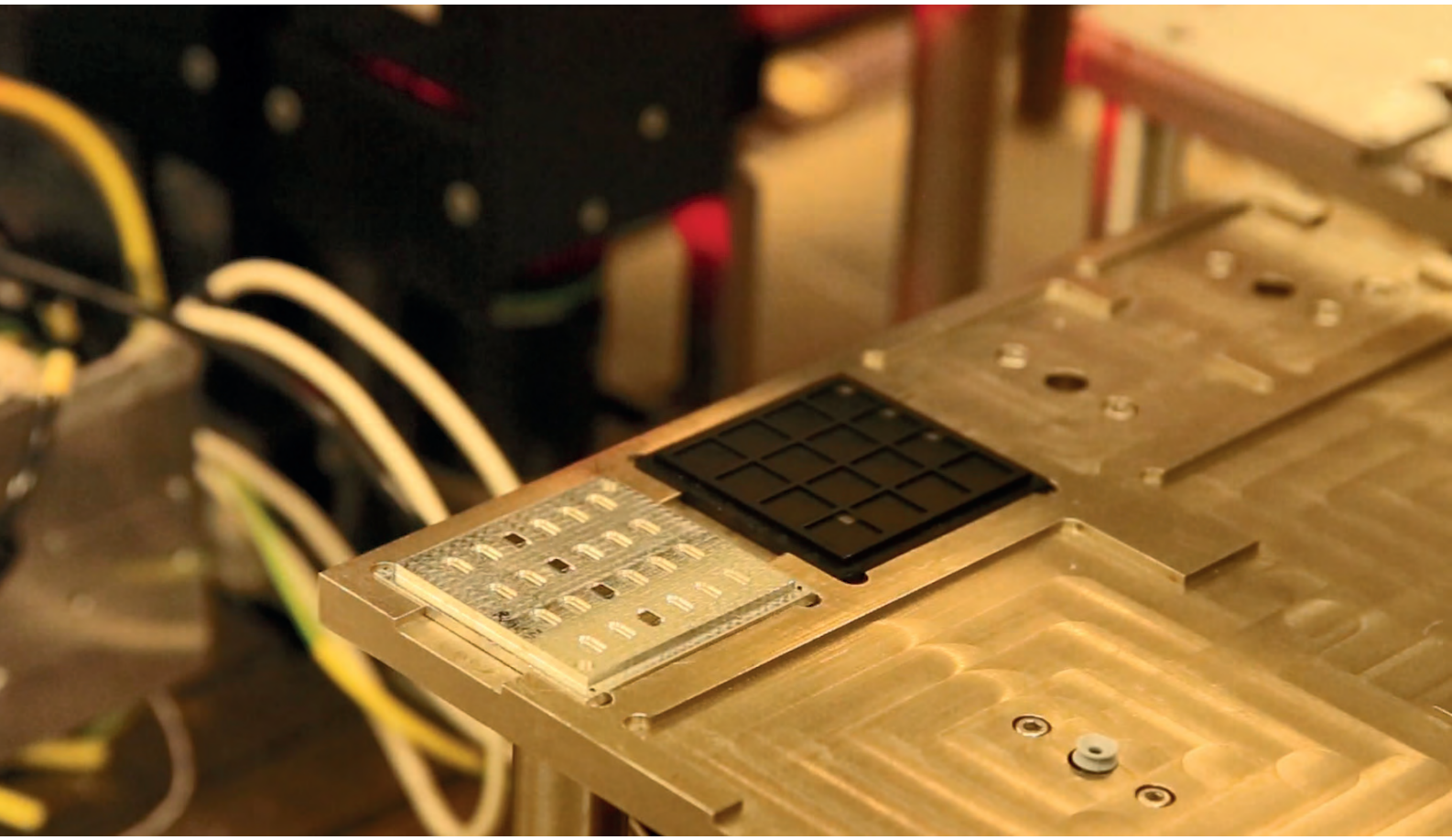


Turbo-charging transmission with digital signal processing

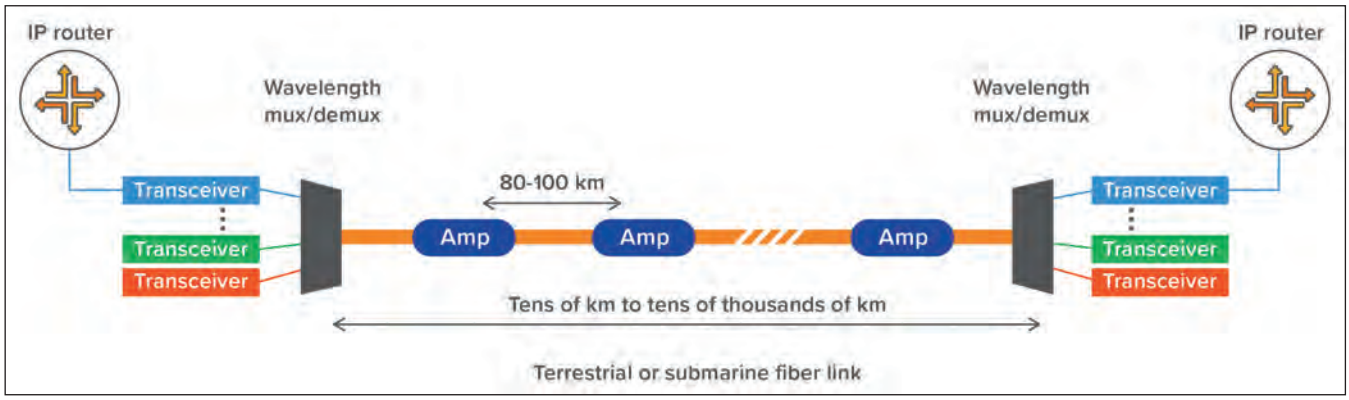
To ease the strain on optical infrastructure, leading communication systems are combining high-quality InP lasers, detectors and modulators with advances in digital signal processing

BY GEOFF BENNETT, YUEJIAN WU, AND HAN SUN FROM INFINERA

KNOWN AS 'Motormouth', the New Yorker John Moschitta Jr., who can hit 586 words per minute in full flow, is generally regarded as the fastest talker in the world. Note that we say 'generally', because two people have gone faster – but when you watch them in slow-motion, you'll see that they make mistakes or are incomprehensible.

Optical transmission shares this problem – that is, as the rate of information transfer increases, so does the difficulty of reliable reception. But, unlike the human ear, designers of optical transmission systems implement powerful digital signal processor (DSP) techniques to clean up the signal and dramatically improve the reliability of data reception. Here, we review the challenges of high-speed transmission, before explaining how Infinera has used DSP to revolutionise optical communication.

Let us begin by considering a simplified long-haul optical transmission link; it could operate between two cities or even under the ocean. For this example, depicted in Figure 1, a pair of IP routers are connected over blue transceivers. At each end, a terminal system multiplexes and demultiplexes optical signals from lasers emitting at slightly different wavelengths, and



directs them down a single pair of fibres. Note that with this well-known technique, referred to as dense wavelength-division multiplexing or DWDM, one fibre usually provides the transmit path and the other the receive path.

A key component within this communication system is the transponder. It receives data from various digital services, including Ethernet connections from 1 Gbit/s to 400 Gbit/s, and maps these bits into a suitable digital container, before converting the digital electronic signal into an analogue one that is sent into a modulator, which in turn controls a laser. The optical pulses coming from this laser, and those used alongside it that are each emitting at a slightly different wavelength, are combined into a single optical fibre.

The great strength of this parallel DWDM approach is that it allows an increase in the total optical fibre capacity independent of the scaling of the individual wavelength data rates. Thanks to this, the DWDM transmission industry has increased total fibre capacity by a factor of 200 in the past 20 years, spurred on by an insatiable desire for ever-higher-speed internet connectivity.

During this tremendous increase over the last two decades, there have been two dramatic jumps around 2009: back then per-wavelength and per-fibre capacity first shot-up by a factor of four, to 40G per wavelength, before then climbing by a factor of 10 or more. Underpinning this expansion, which marked an inflection point in optical capacity growth, came a move to coherent transmission with advanced digital signal processing. Since then, per-wavelength data rates have steadily increased by another factor of eight, with current leading-edge products operating at 800 Gbit/s.

Prior to 2009, long-distance transmission tended to involve simple on/off keying in the transmitter. At the other end of the fibre, a direct photodetector converted this very 'binary-looking' modulation back into an electrical signal. We refer to this form of transmission as intensity modulation with direct detection. One of its key traits is that it features a direct detector, operating on a square law relationship to the strength of the received modulation symbols. By taking this approach, it is very difficult to use digital signal processing to compensate for linear optical impairments, issues that we will now outline.

Figure 1. Elements of a typical long-haul or submarine optical network link.

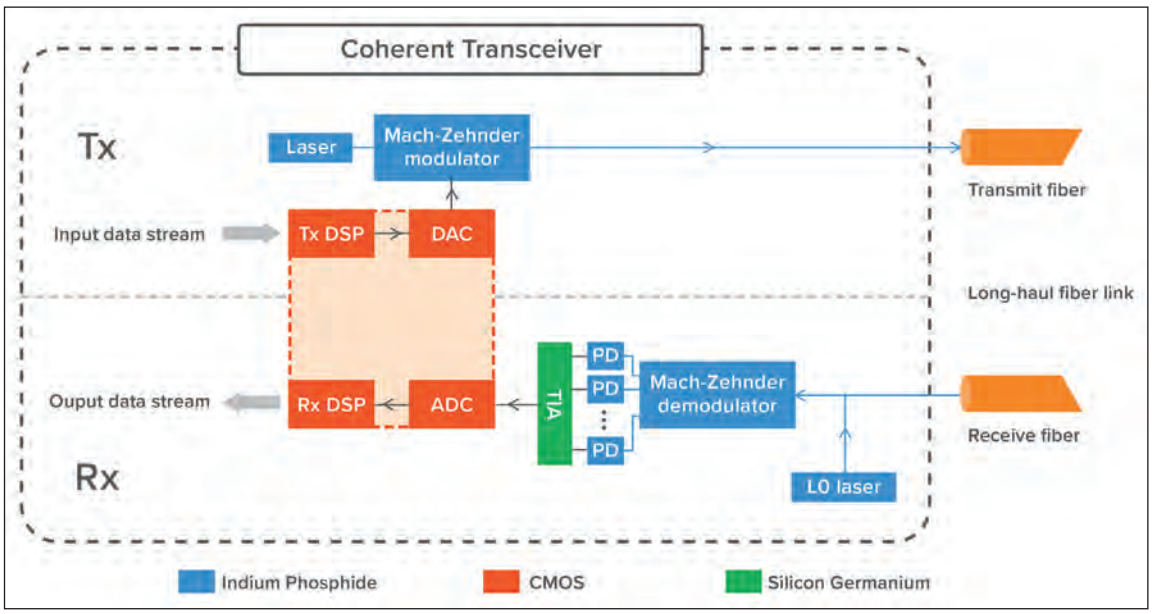


Figure 2. Schematic of coherent transceiver showing transmit and receive DSP location.

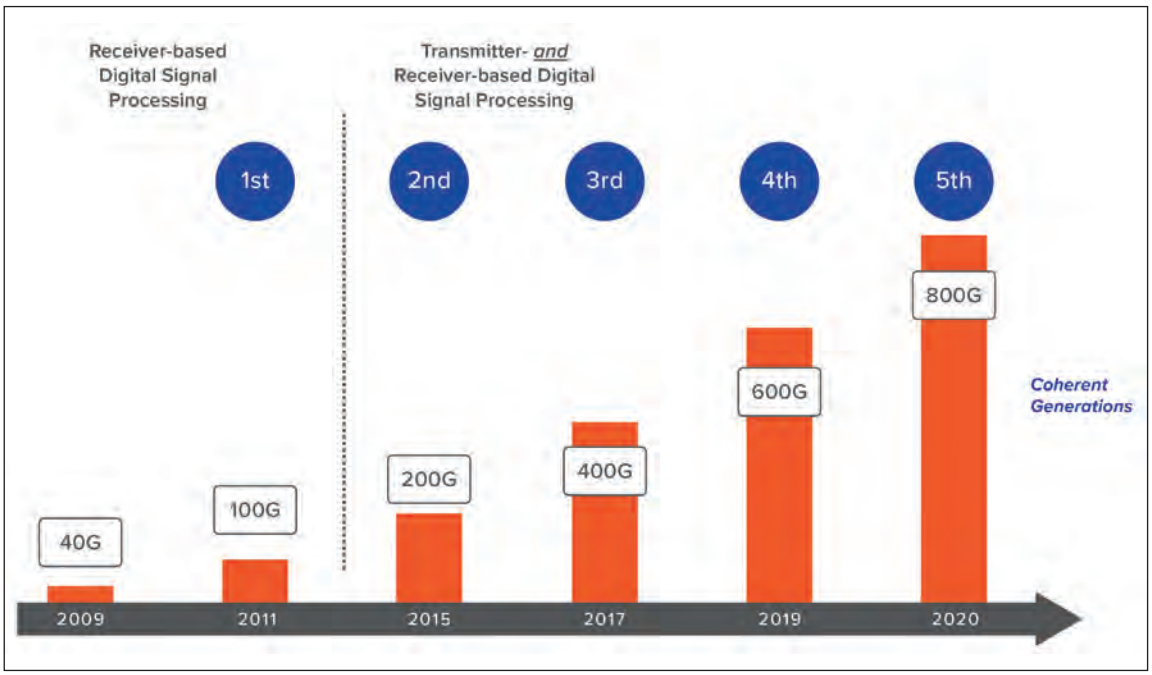


Figure 3. Evolution of headline data rate for coherent transmission.

Just as John Moschitta's rivals introduced 'noise' – that is, errors – into attempts to break the words-per-minute record, an optical fibre link can suffer from noise that comes from a number of different sources. As production methods evolve, some of these improve over time, such as the quality of the laser and the noise level of the amplifiers.

Other signal distortion effects can be compensated for with powerful mathematical techniques, so long as we can implement a linear detector. These include: dispersion effects, particularly chromatic dispersion and polarization-mode dispersion; high-order modulation issues, which can be addressed using a technique called probabilistic constellation shaping; and nonlinear effects, which are triggered by high optical power levels in the fibre.

The first of these, dispersion, is associated with the spreading out of the modulation symbol on its journey along the fibre. If you fail to reverse that effect, the sequential symbols will run into one another, preventing the receiver from correctly interpreting the value of a given symbol. This is analogous to one of Moschitta's rivals slurring their words, so that they run together, making it harder to understand where one word ends and another begins. Chromatic dispersion stems from the different frequencies of the modulation symbols, while polarization-mode dispersion comes from the vertical and horizontal polarizations of the modulation symbol travelling at slightly different speeds.

High-order modulation involves cramming more bits into a single modulation symbol. It is a bit like Moschitta's rivals talking more quickly, which makes it more difficult to understand them. One way to view the solution, probabilistic constellation shaping, is that it is like having a way to deliberately choose words that sound very crisp and clear when they are said one after the other. This is clearly preferable to words that mean the same thing, but are harder to distinguish in a given set of words.

Non-linear effects, the third form of signal distortion that we list, are introduced when the optical power level in a fibre exceeds a certain threshold. This issue is similar to that of Moschitta's rivals talking into the microphone so loudly that the listener starts to hear distortion.

Coherent optical transceivers

In 2010 the optical industry began to deploy a radically different approach for sending and receiving information – phase modulation with coherent detection (see Figure 2 for a simplified schematic of the latest generation of coherent transceiver). While the first generation of coherent transceivers had processing only in the receiver, subsequent generations include both transmitter and receiver-based processing.

The laser in the transmitter shines constantly – creating an optical carrier. The digital electronic signal is sent into the transmit portion of the DSP for pre-processing, then the processed digital signal is sent to a high-speed digital-to-analogue converter (DAC), with the resulting analogue signal applied to a Mach-Zehnder phase modulator, which applies this signal to the optical carrier. Note that by sending separate modulation signals on the X and Y polarizations of the light, the capacity of the modulation symbol is doubled. After this, the optical signal, containing a stream of high-speed modulation symbols, is launched into the fibre for its journey of many kilometres.

Within the receiver, there is a local oscillator laser with a continuous output, tuned to the wavelength to be received. The local laser output is mixed with the incoming signal from a fiber, and the mixed signal is then split into X and Y polarizations. The parallel signals enter a phase demodulator array, formed from adjustable Mach-Zehnder elements. This results in the generation of a massively complex set of interference patterns that would be changing so quickly they would appear as a constant light to the human eye. A parallel set of photodetectors captures the interference patterns, converting the analogue optical signals to analogue electrical signals that are boosted by a transimpedance amplifier. These stronger signals are sampled and digitized in an analogue-to-digital converter (ADC), with the resulting digitalised signal passed to the receiver DSP and processed to produce a clean, reliable bit stream.

Unlike a pure electronic circuit, the optical transceiver makes use of a range of semiconductor materials, using the most appropriate one for each task (these materials are colour-coded in Figure 2).

Regular readers will know that InP is the ideal material for creating high-performance lasers and photodetectors at wavelengths employed for long-distance optical transmission, typically the domain that spans 1530 nm to 1625 nm. InP is also the best choice for the modulators at these data rates. Due to this dual role, it is possible to use InP for all the optical functions for both transmit and receive, forming a single photonic integrated circuit (PIC). SiGe is the material used to produce transimpedance amplifiers that deliver consistent amplification over wide bandwidth and a low noise level, while silicon CMOS is employed for making application-specific integrated circuits (ASICs) used for the DAC, ADC, and DSP functions. In Figure 2, we show that the transmit and receive DSP circuits are implemented on a single ASIC chip. Using this architecture, at least one of the latest 800 Gbit/s implementations is made up of more than 5 billion transistors.

Materials aside, those of you with a background in radio communication will be familiar with the approach that we shall now describe. At the transmitter, instead of sending an on/off signal, we use a phase modulator to encode digital signals as a set of different phase states. And at the receiver, rather than directly interpreting the on/off signal without any processing, we use a coherent detector – this consists of a reference laser, known as the local oscillator, the signal of which is mixed with the data signal. When used in radio systems, a local oscillator allows tuning in to a specific radio station, out of perhaps dozens of radio stations that have signals passing through the detector.

In optical transmission, the situation is slightly different, as we have already separated the particular wavelength we wish to receive. In this case, the local oscillator acts as a very low-noise amplifier, and the resulting phase demodulator is a linear detector. Having a linear detector is a tremendous asset, allowing us to finally bring the power of digital signal processing to bear on the problem of compensation of linear channel impairments such as chromatic dispersion and polarization-mode dispersion.

Advancing DSPs

While coherent detection may be familiar to anyone from the radio world, and DSPs to fans of DAB radios, the sample rates and processing power required to process high-speed optical signals are on a totally different scale. To put this in perspective, for CD quality audio the accepted sample rate is 44.1 kHz, while a modern coherent transponder operates about two million times faster at well above 100 GHz sampling rate to correctly recover transmitted information from signal symbol rates close to 100 gigabaud.

In the 1970s, the first hardware used for digital signal

processing emerged. It employed general-purpose processors, with a software implementation. The processors were clocked at about 2 MHz, with four clock pulses per machine cycle. Even five decades on, armed with tremendous advances in processor performance, dedicated chips for DSPs are still essential. That's partly due to performance demands, but also associated with the need to reduce power consumption, size, and hardware costs. For coherent processing, sample rates have to be somewhat higher than the symbol transmission rate – a requirement first explained by Bell Labs researcher, Harry Nyquist, in the 1940s, in the context of digital telephony.

The key to realising the processing rates needed for high-speed optical transmission is to use the very latest process node sizes for a given coherent generation. Progress is fast, evolving from 100 Gbit/s transponders with around 300 million gates in 2010 to 800 Gbit/s today, using over 5 billion gates (see Figure 3 for the impact of this evolution on wavelength data rates).

One downside of coherent processing is that it consumes a significant electrical power budget. Consequently, in order to maintain stable operation, heat must be pulled from the chips. Historically, Moore's Law is to thank for providing a pathway to reducing electrical power, per unit processing power. While there are various forms of this law, they all refer to a trend of doubling certain chip metrics within a given time period. This advance leads to a faster processing at lower power. In the case of the ASIC technology used in coherent DSPs, as each generation of process node delivers roughly a 0.7 times reduction, two generations of progress are needed to double the DSP bandwidth for the same power consumption.

Improvements are now more challenging. The recent move from 16 nm feature sizes in fourth-generation transceivers to 7 nm in the current fifth-generation transceivers delivered around a 51 percent saving in power consumption per unit processing speed. In comparison, there will only be a power saving of around 30 percent when moving from 7 nm to 5 nm.

Detailed predictions of likely developments in electronic devices and systems are presented in the *IEEE International Roadmap for Devices and Systems*. One of the goals of this roadmap, which includes the ASIC technology used for DSPs, is to identify key trends related to devices, systems, and all related technologies over the next 15 years. Additional aims are to determine generic devices' and systems' needs, challenges, potential solutions, and opportunities for innovation; and to encourage related activities worldwide through collaborative events, such as related IEEE conferences and roadmap workshops.

Right now, there is no clear solution to the slowing down of power reduction. An imperfect option would be to design a MOSFET with a steep sub-threshold, but while this would result in more efficient power consumption, it would go hand-in-hand with a slower processing rate for serial operations within any pathway through the DSP. The general consensus within the semiconductor community is that a new DSP architecture is required to maintain the historical rate of progress.

Capacity challenges

Valuable contributions from Bell Labs to the development of DSP are not limited to the work of Harry Nyquist. Contemporary Claude Shannon made

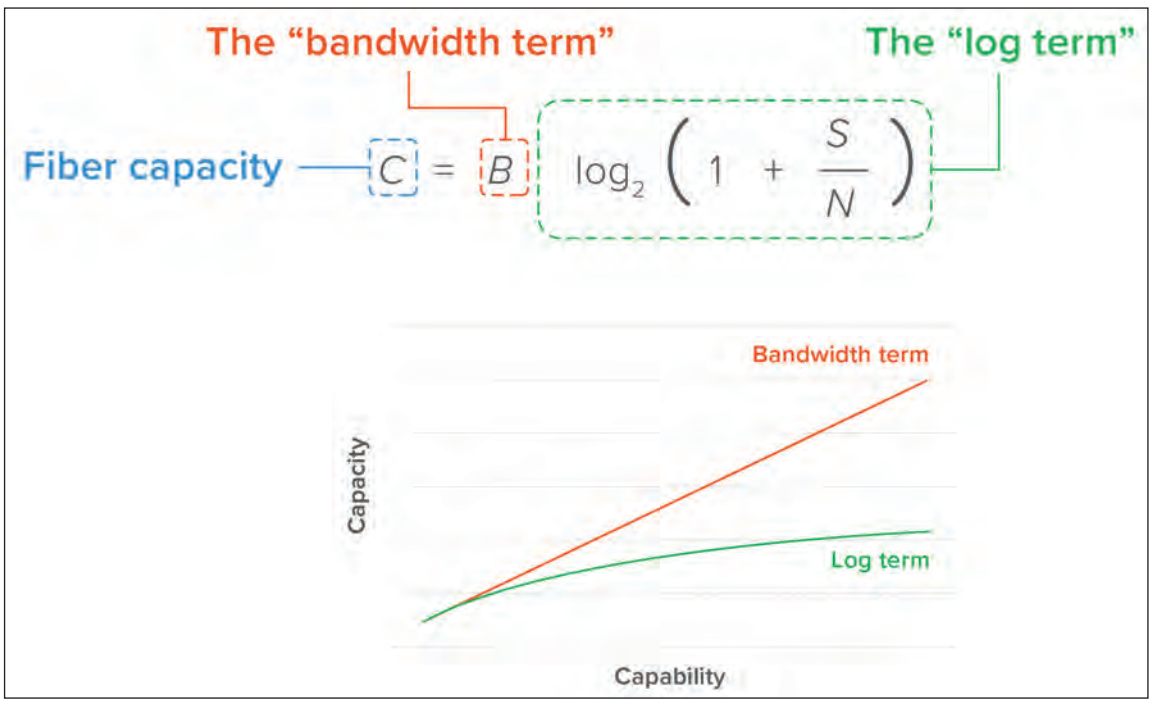


Figure 4: The Shannon equation and the diminishing returns in fiber capacity from future coherent transceiver enhancement

other contributions to information theory, including developing an equation that allows us to calculate the maximum capacity for a given communication channel. Back in the 1940s, Shannon would have been thinking of a copper telephone wire or wireless telegraphy channels, but now, in the era of optical communication, it is used when considering optical fibres.

The Shannon equation, in simplified form, is shown in Figure 4. On the left is *C*, representing the channel capacity, and on the right are two terms: one represents the bandwidth of the channel, and the other is related to the signal-to-noise ratio. For optical transmission, the bandwidth is the range of wavelengths used for amplifying the signals as they travel along the fibre. This is usually the C-band, which spans 1535 nm to 1565 nm, and may sometimes also include the L-band, which is the domain from 1565 nm to 1625 nm. Within the log term, there is a function based on the signal (*S*)-to-noise (*N*) ratio, which is often summarized as 'bits per channel utilization'.

Included in Figure 4 is an illustration of how channel capacity, shown on the vertical axis, increases for a given rate of improvement in either the bandwidth or *S*/*N* ratio. There is a better return for increases in bandwidth, because *S*/*N* is within a log function, so improvement in capacity tails off. This implies that there are diminishing returns when efforts are directed at improving amplifier noise levels, fibre quality, and in particular coherent modem functionality, because they all address the *S*/*N* ratio.

The good news is that there are a range of options for increasing bandwidth. Consider, for example, the C-band. Bandwidth can be increased by turning to Super C-band amplifiers – this boosts amplified bandwidth by a little over 20 percent – and also by using the L-band (note that the L-band is almost never deployed on its own – it is always deployed with C-band). Compared to a conventional C-band system, one that amplifies Super C- and Super L-bands delivers almost three times the bandwidth.

These options are focused on terrestrial networks, where it is relatively easy to deliver electrical power to an amplifier chain. That's not the case in submarine cables, which contain a thick conductive layer that delivers up to 15 kV to each end, to power the amplifier. In a submarine cable, it is often the ability to deliver power to an amplifier chain that limits the number of fibre pairs.

An alternative submarine cable architecture, now being deployed in some newer cables, is space-division multiplexing. As this reduces amplifier power consumption, it sacrifices capacity per fibre pair, but trades this for an increase in the number of fibre pairs. The change is beneficial, increasing the capacity for the cable. An additional move in this direction is the evolution of coherent transponders, which are expected to limit the additional optical performance in exchange for a smaller module size with lower power consumption. This process will be driven by 5 nm or smaller DSP process nodes.

Whether the networks are terrestrial, or they run along the sea bed, there is plenty of scope to maintain optical transmission capacity in the short to medium term.

For the past decade, high-speed optical transmission has relied on the power of advanced digital signal processing to increase data rates per wavelength, and ultimately the total fibre capacity of long-distance and submarine communication systems. While there are challenges to both DSP scaling and fibre transmission limits, strategies and solutions are available for maintaining growth in capacity, while driving down the cost of moving information around the world.

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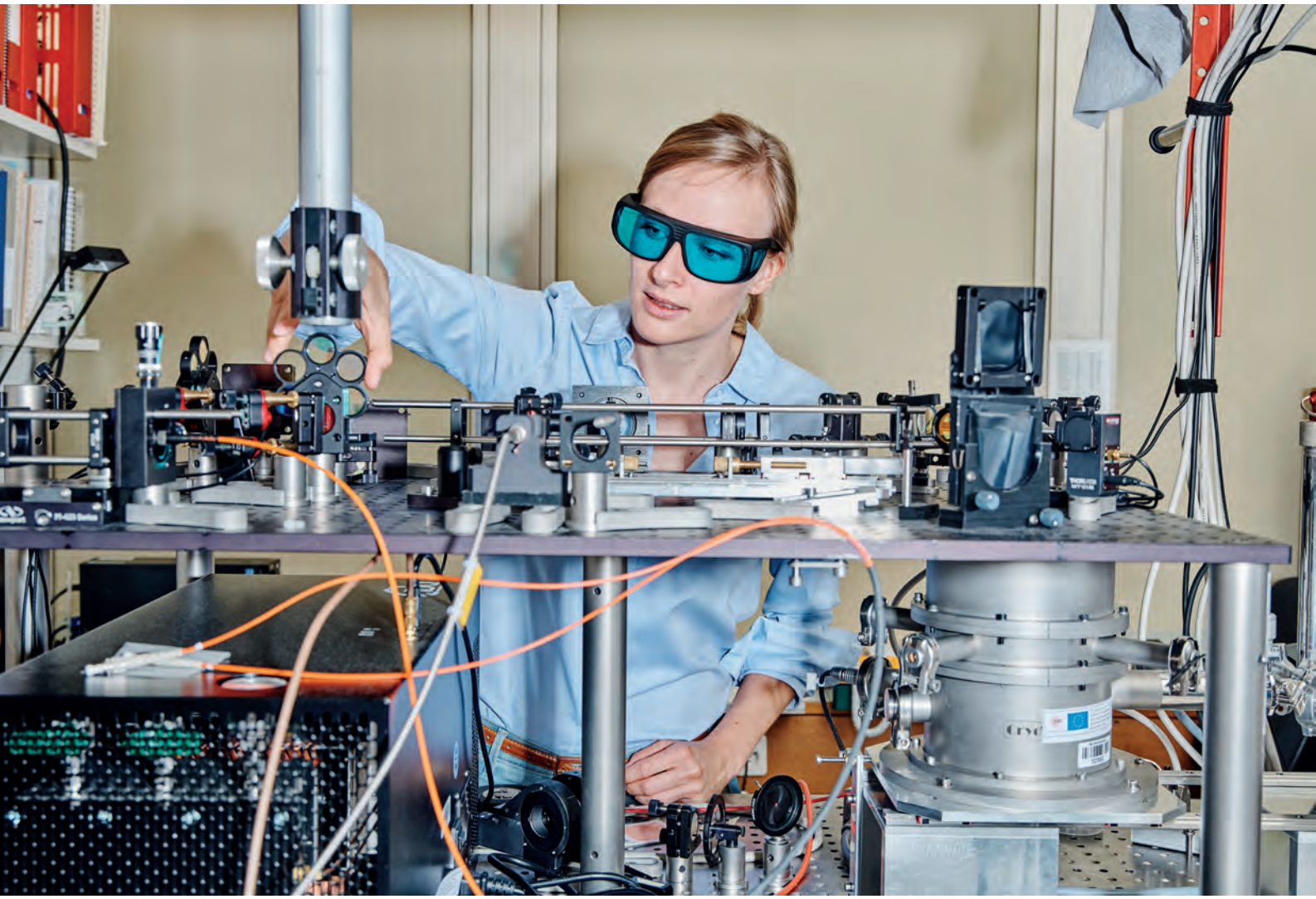

Self-aligned growth spawns hybrid photonic devices

Miniature, high-performance optical links could be formed on silicon substrates through self-aligned growth in oxide tubes

BY SVENJA MAUTHE, NOELIA VICO TRIVIÑO, MARILYNE SOUSA, HEINZ SCHMID AND KIRSTEN MOSELUND FROM IBM RESEARCH EUROPE

SILICON MICROELECTRONICS has made staggering progress. The latest components have a footprint of just a few tens of square nanometres, consume very little power, and are packed in their billions on a chip.

Today's technology, the culmination of decades of silicon CMOS processing development, has also spawned advances that benefit silicon photonics. Fabs can now produce low-loss silicon waveguides and passive structures to route optical signals through a chip. However, this technology is not perfect. Arguably its biggest weakness is the lack of optical gain, stemming from silicon's indirect bandgap.

Free from this limitation are a portfolio of III-V compound semiconductors with direct bandgaps

spanning the entire spectral range from the visible, using III-nitrides, to the near infrared (see Figure 1). The latter is of interest for optical communication, with bands around 1350 nm and 1550 nm – they are known as the O-band and C-band – providing the preferred choices for datacom and telecom, respectively. These bands have been adopted because they correspond to minimum transmission losses in optical fibres, and coincide with the availability of effective sources and erbium-doped fibre amplifiers (EDFAs). These spectral domains are also well suited for on-chip applications, thanks to silicon's transparency at wavelengths beyond 1.1 μm. Due to this attribute, SOI waveguides can serve as a low-loss transmission medium.

An additional attribute of the ternary or quaternary III-Vs is that by adjusting their composition, the bandgap is varied, enabling the growth of quantum wells and dots. Consider, for example, the combination of InP and $In_{0.53}Ga_{0.47}As$, a pairing that share the same crystal lattice constant, enabling defect-free growth. The bandgap of $In_{0.53}Ga_{0.47}As$ is just 0.74 eV, far less than the 1.35 eV for InP, so inserting an $In_{0.53}Ga_{0.47}As$ layer between InP barriers creates a deep potential well that excels at confining excited electrons and holes and localising the recombination process. The opportunity to form quantum wells and quantum dots has been instrumental to the development of today's efficient III-V lasers.

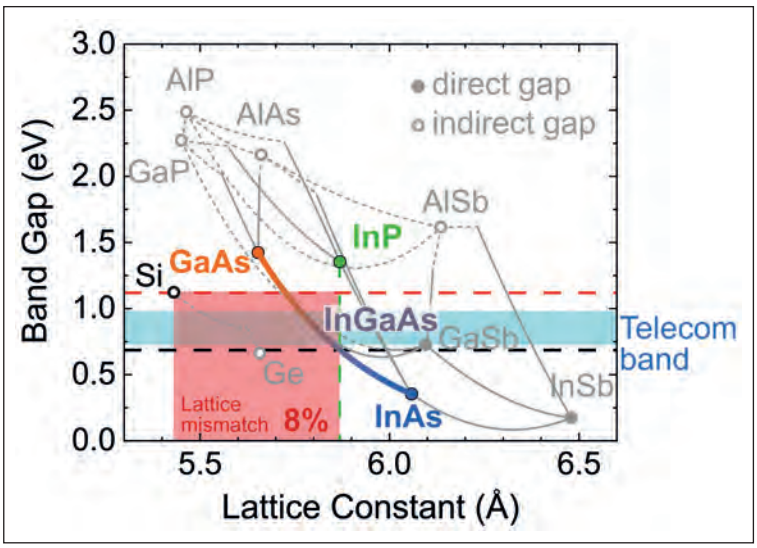

Figure 1. Bandgap versus lattice constant for a variety of direct (full circle) and indirect (circle) semiconductors. The 8 percent lattice mismatch between silicon and $In_{0.53}Ga_{0.47}As$ is highlighted. The blue shaded area corresponds to the telecommunication band.

Uniting III-Vs and silicon

One of the holy grails of research within the semiconductor industry is the seamless integration of photonics and electronics, so engineers can draw on the best of both worlds. Today, the state-of-the-art approach to accomplishing this is to directly bond a wafer with a III-V active stack onto a pre-processed silicon wafer (see Table 1, which compares this approach to other techniques for integrating III-Vs on silicon). Wafer-bonding allows light to couple evanescently from underlying silicon waveguides to the active III-V regions above. Engineers have demonstrated highly advanced devices with this approach, integrating both detectors and lasers.

Bonding can also take place at the die level. In this case, individual III-V dies or pre-processed III-V devices can be united with a silicon platform. While these chips may seem small from the perspective of the III-V community, with dimensions of several

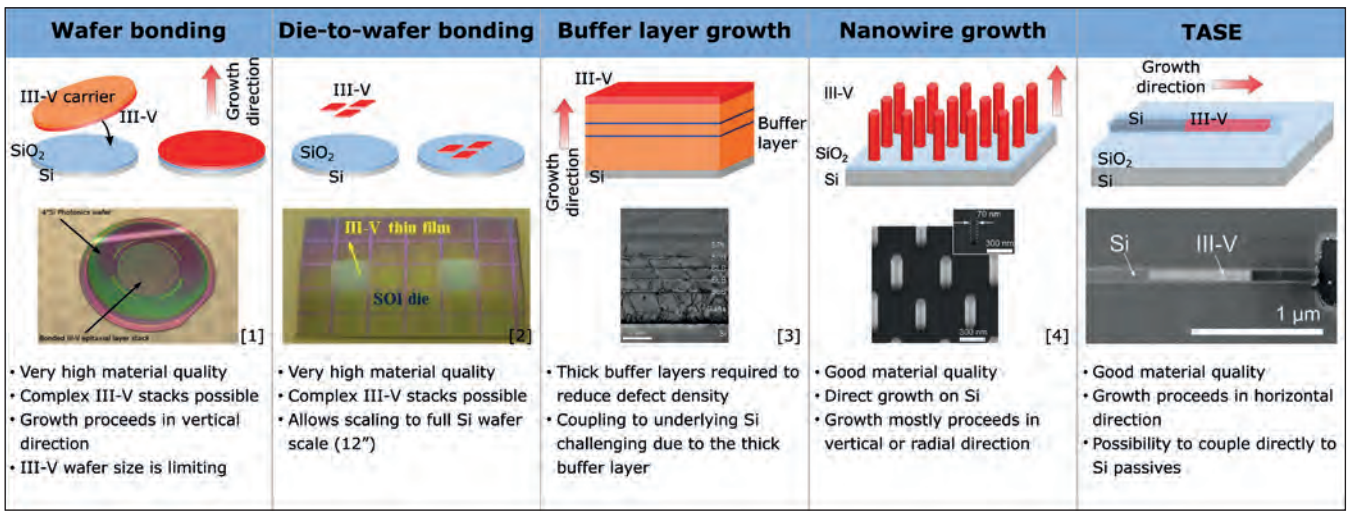

Table 1: Overview of existing technologies for integrating III-V materials on silicon. Reprinted with permission from [1] M. Seifried *et al*. IEEE JSTQE **24** 8200709 (2018), doi: 10.1109/JSTQE.2018.2832654, licensed under CC BY 4.0; [2] S. Keyvaninia *et al*. Opt. Mater. Express **3** 35 (2013), doi: 10.1364/OME.3.000035, ©2012 Optical Society of America; [3] I. Luxmoore *et al*. Sci Rep **3** 1239 (2013), doi: 10.1038/srep01239, licensed under CC BY-NC-ND 3.0; [4] T. Katsuhiro *et al*. J. Phys. D: Appl. Phys. **47** 394001 (2014), doi: 10.1088/0022- 3727/47/39/394001, ©2014 IOP Publishing Ltd, CC BY 3.0.

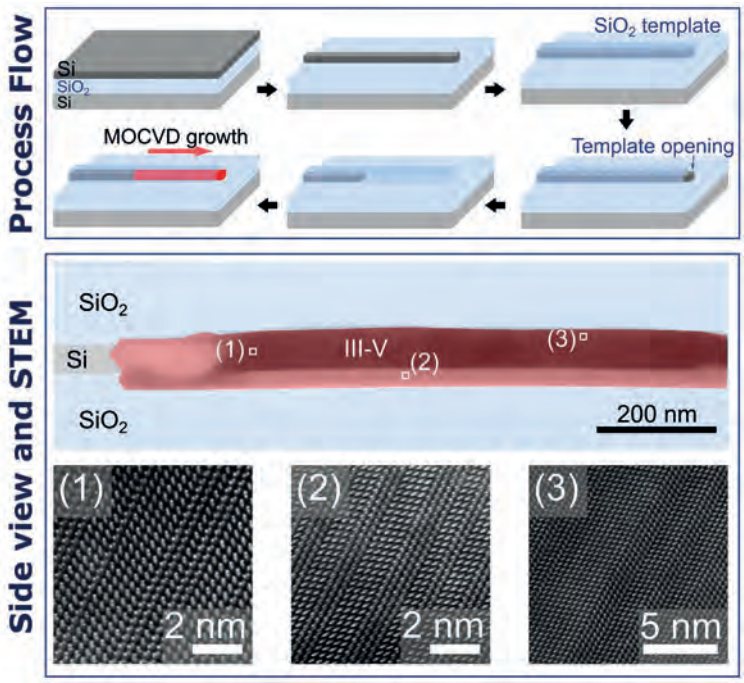

Figure 2. Template-assisted selective epitaxy (TASE) process flow and material investigation using scanning transmission electron microscopy (STEM). TASE is performed on an SOI wafer. The top silicon surface is patterned and covered with SiO_2. Subsequently an opening is etched into the oxide shell on one side and the underlying silicon is partially etched. Using MOCVD, III-V material is grown from the remaining silicon into the empty SiO_2 tube. Images reprinted with permission from S. Mauthe *et al*. Nat. Commun. **11** 4565 (2020).

hundred microns, they are far, far larger than electronic components. With transistors typically fitting within tens of nanometres, the size mismatch is about three orders of magnitude.

Gaining in popularity, monolithic growth offers another option for uniting III-Vs with silicon. This approach enhances integration densities, by depositing III-V material locally, only where it is needed. While this method has much appeal, its execution is challenging, partly because there is significant difference in atomic spacing of the respective crystal lattices (see Figure 1). For example, there is a lattice mismatch of about 8 percent between silicon and InP/$In_{0.53}Ga_{0.47}As$. This difference can result in numerous dislocations and anti-phase boundaries that hamper the performance of optical devices. Adding to the challenges of monolithic growth, different materials can have different thermal expansion coefficients, causing cracks and defects to appear when cooling the wafer down from its growth temperature, typically 550 °C to 700 °C, to room temperature.

A well-known approach to overcoming both these issues is to switch from growing a stack of layers to growing nanowires. The growth of III-V nanowires can begin with a metal catalyst (usually vapor-liquid solid type growth), or with an opening defined in a pre-patterned hard-mask on the surface of a silicon wafer, and approach known as selective-area epitaxy.

Our team at IBM Europe has trailblazed yet another technique for marrying III-Vs with silicon. Our approach, which we refer to as template-assisted selective epitaxy (TASE), involves the growth of III-Vs within oxide tubes formed on a silicon substrate (see Figure 2 for an outline of the process flow).

In our case, growth of the III-V begins with nucleation on a small silicon surface, exposed at one extremity within the hollow template. Just like the formation of nanowires, growth is monocrystalline, with typical defects from heteroepitaxy suppressed. We can produce larger or more exotic shapes by adapting the size of the template – however, for the work we discuss here, we only fabricate simple bars or nanowires. Unlike conventional nanowires, our structures are grown along the surface of silicon, enabling integration with photonic silicon structures.

It is interesting to note, however, that we did not develop TASE for photonics. Initially, we targeted electronic applications, using this technology to provide a complementary tunnel FET platform, which is described on pages 38 to 42 of the January/February 2017 edition of *Compound Semiconductor*.

There are two essential attributes of our TASE technology that enable us to form the devices described in the remainder of this article. Firstly, because our method relies on replacing existing silicon features by a III-V, it is self-aligned – the shape and position of the compound semiconductor material that we add is defined in the same lithographic step as the silicon features. Thanks to this, we can perfectly tune the coupling to waveguides, and we can insert scaled III-V features within a silicon photonic crystal lattice. The upshot is that we engineer truly hybrid structures, integrated seamlessly. Secondly, we can introduce doping profiles and composition gradients *in-situ*, during growth. One of the merits of the geometry that results from our process is that it makes coupling to silicon waveguides straightforward.

Monolithic detectors

As optical signalling extends from server racks to on-board and finally on-chip schemes, demand for detectors will grow to thousands, if not millions. While an on-chip light source is highly desirable but not mandatory, densely integrated photodetectors are an essential ingredient in optical transceivers, required to process the incoming optical signal.

To successfully replace lossy electronic interconnects, it is critical that power-consumption is at the very least similar – and ideally lower – than that of comparable electronic interconnects. Efforts must focus on limiting RC constants, a requirement that can be accomplished with small-footprint devices with small capacitances. The key to satisfying these constraints

is to transition away from today's large, high-performance devices – and this is where III-Vs have an important role to play.

Today's state-of-the-art integrated detectors are based on SiGe, a common alloy in CMOS technologies. As this binary material has an indirect bandgap, absorption is lower than for a corresponding direct bandgap material. While the widespread adoption of silicon CMOS image sensors amply demonstrates that it is perfectly possible to make excellent detectors with SiGe, a detector with a direct bandgap might be even more efficient. Introducing III-Vs not only boosts efficiency – it also opens the door to miniaturisation of the active region and, in turn, a trimming of device capacitance.

Another reason for embracing the III-Vs is that SiGe compounds do not span an ideal absorption range. They make for excellent detectors in the visible, and can reach the O-band at around 1350 nm by increasing the germanium concentration, but the important 1550 nm wavelength is very close to the detection limit.

Recently, we demonstrated the first InGaAs photodetector that is monolithically integrated in-plane on silicon, growing the device from a silicon fin. From a photonics perspective, this might be viewed as a butt-coupling approach. We focused on improving speed and power efficiency through scaling. To this end, we kept geometries small, limiting height to only 60 nm. As this is insufficient for sustaining a propagating mode in the near-infrared, we turned to free-space fibre coupling for device characterisation.

Our devices exhibit impressive characteristics. Dark current is low, while estimated responsivity hits 0.65 A/W. As our free-space coupling prevents a direct measurement of responsivity, we calculated this value, assuming that only the photons absorbed in the intrinsic region contribute to the photocurrent, which is an ideal case scenario.

To demonstrate the potential of our technology for high-speed data transmission, we have recorded eye diagrams. They show that we can distinguish '0' from '1' at data rates up to 32 Gbit/s, the limit of our experimental setup. These results, illustrated in Figure 3, shows a f_{3dB} of about 25 GHz in the frequency response curve. While these results are encouraging, even better ones should follow. Opportunities for further progress include introducing an improved contact and layout scheme and optimising the resistive components of the devices.

Another attribute of our devices is that they deliver a promising spectral response. They show maxima of detection in both the O- and C-band regions, with the peak in the O-band being the strongest. According to TCAD simulations by our collaborators at ETH Zurich, our detector's spectral response is linked to device design and geometry, factors that need to be considered when designing scaled photonic components.

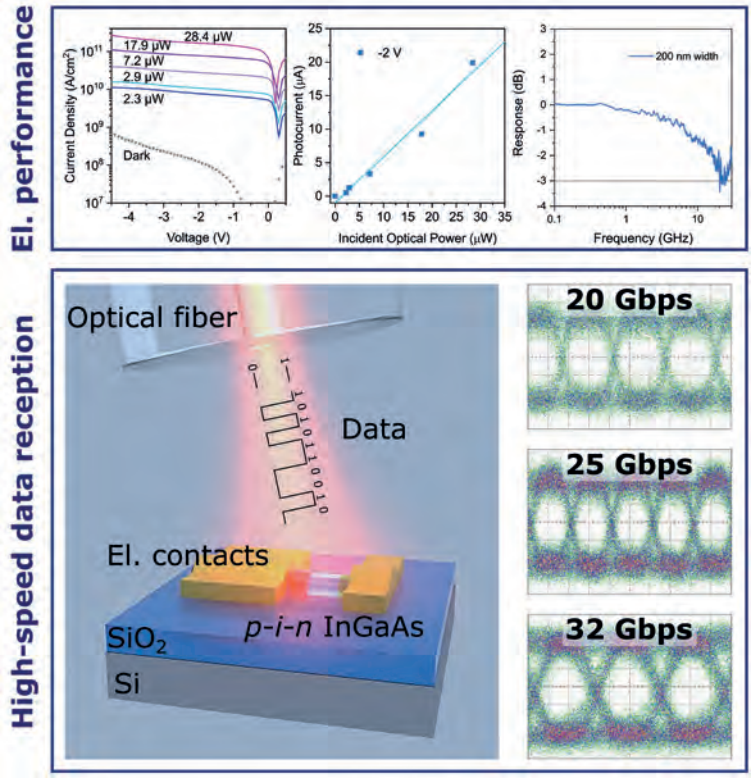

Figure 3. Overview of electro-optical performance of a scaled, TASE-grown photodetector with 200 nm width. The top part of the image depicts a typical diode-like current-voltage (IV) curve on the left-hand side. Under light illumination, a photocurrent flows, increasing with illumination power. Plotting the measured current under reverse bias as a function of the incident light illumination reveals a linear relationship, suggesting a high responsivity (see middle image). On the right-hand side, the S_{21} response measurement is depicted. The line at -3 dB marks the 3-dB limit. The lower part depicts the high-speed data reception measurements. As illustrated, an optical fibre is aligned free-space and light modulated onto the device. The three images on the right depict the measured eye diagrams with open circles up to 32 Gbit/s. Images reprinted with permission from S. Mauthe *et al*. Nat. Commun. **11** 4565 (2020).

Hybrid photonic crystals

Our ultimate goal is to fabricate a fully integrated optical link. To realise this, we need to develop an on-chip laser or emitter. We are pursuing a photonic crystal architecture. This is a promising option for anin-plane light source, because it has the potential to combine high efficiency with low power and miniaturisation, thanks to a high quality factor and a small mode volume.

Most photonic crystal structures are two-dimensional or one-dimensional lattices, created by etching holes in a dielectric material or by stacking densely placed rods or fins. The latter architecture can be directly integrated with our TASE technology, which we developed for the detectors. Following in the footsteps

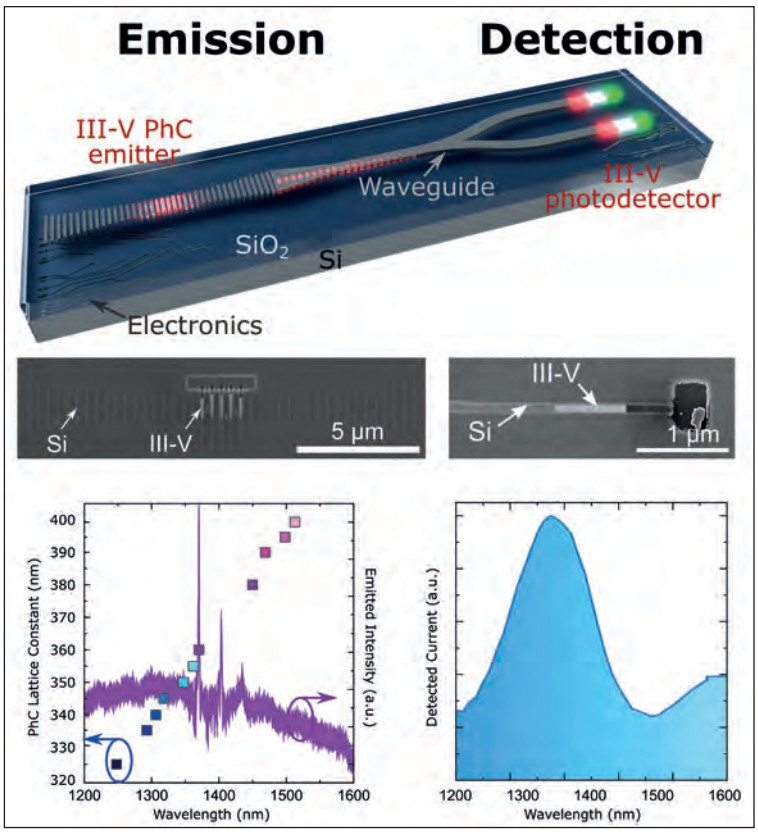

Figure 4. Vision of a TASE platform for integrated optical links. The top image shows the envisioned optical link with a photonic crystal (PhC) cavity emitting light directly into a waveguide. The waveguide is coupled to detectors to detect the emitted light. In the centre, two scanning electron microscopy images depict a fabricated photonic crystal cavity and a photodetector, respectively. The bottom two images depict the spectral performance of the emitter and detector, respectively. The images are reprinted with permission from S. Mauthe *et al*. Nat. Commun. **11** 4565 (2020) and S. Mauthe *et al*. Nano Lett. **20** 8768 (2020).

of our process for making detectors, we etch back the silicon in a selected number of rods, prior to re-growth of the III-V. This is a straightforward approach to creating a hybrid structure, where most of the photonic crystal cavity consists of plain silicon – III-V is only present in the central region of the cavity.

With this design, the InGaAs emits in the near-infrared, above the silicon absorption edge. At this wavelength the silicon part of the photonic crystal cavity is transparent. By only using gain material where essential, we trim optical losses, leading to a substantial improvement in the final device performance. It is a non-trivial task to design a photonic crystal structure with a high quality factor. Helping with this endeavour, we recycle existing designs, replacing just an important segment of the cavity with III-V while retaining the remaining features in silicon.

Our hybrid photonic devices produce tuneable light emission across the telecommunication band. They offer many valuable characteristics: they feature high yield and robustness, with similar experimental Q-factors in excess of 1000; and controllable cavity emission wavelengths, despite some fabrication imperfections. We attribute their strengths to the hybrid concept, which at its heart has the placement of III-Vs at just the desired locations within the photonic crystal silicon structure.

The individual III-V photodetectors and optically pumped photonic crystal light sources that we have demonstrated provide great stepping stones towards our long-term goal of a fully integrated optical link. Our efforts are now being directed at developing a larger waveguide-coupled version of our detector that will allow direct on-chip coupling to integrated lasers. If our optical link is to make an impact, it must also feature light sources that are electrically actuated, rather than optically pumped. That is an extremely challenging requirement for miniature devices – so-called nanolasers or nanoLEDs – as the presence of metals in the vicinity of the optical mode invariably leads to losses, and this inevitably increases the threshold.

We believe that our *in-situ*, in-plane doping process holds the key to producing tiny, electrically pumped emitters. We have already embedded the appropriate composition and doping profile in the III-V rods, and our next step is to add contacts to the ends of these rods, to enable electrical actuation. However, while the next step is clear, implementation is going to be challenging. We can expect a fair bit of engineering to optimise design and accurately integrate low-resistance electrical contacts without destroying the optical mode.

In some ways, the use of TASE is a paradigm shift in the design of nanophotonic devices. Like any new technology, there are challenges – but there are also completely new opportunities, just waiting to be explored.

This work received financial support from European Research Council ERC StG PLASMIC under grant agreement no. 678567 and from Swiss National Science Foundation SNF Spark under grant agreement CRSK-2_190806.

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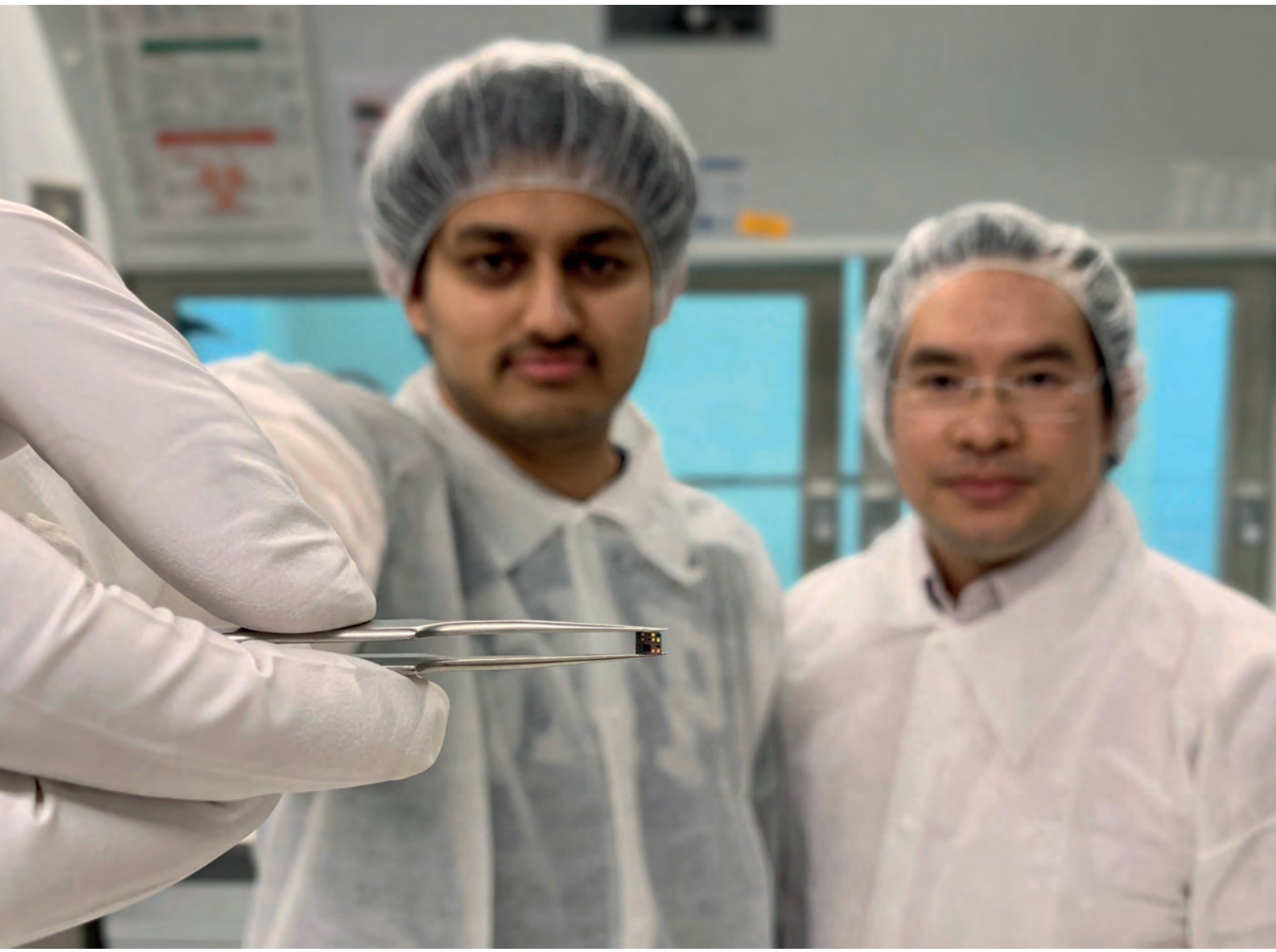

New nanowires spawn superior UV LEDs

Switching from AlGaN nanowires to those made from AlInN offers an attractive route to increasing the output of the UV LED

BY RAVI TEJA VELPULA, BARSHA JAIN, AND HIEU PHAM TRUNG NGUYEN FROM NEW JERSEY INSTITUTE OF TECHNOLOGY

The outbreak of the deadly SARS-COV-2 virus has thrown the UV source into the spotlight. Those emitting deep within the UV, in a domain stretching from 222 nm to 207 nm, can kill this virus and many others, and also deliver surface disinfection. In addition, there are related applications for deep UV radiation, such as water disinfection, that use this source to disrupt DNA and RNA molecules.

As well as this class of application, UV sources can take on many other important tasks: they can be employed for a wide range of UV curing applications, including those involving coatings, inks, adhesives, composites, and stereolithography; they can be used

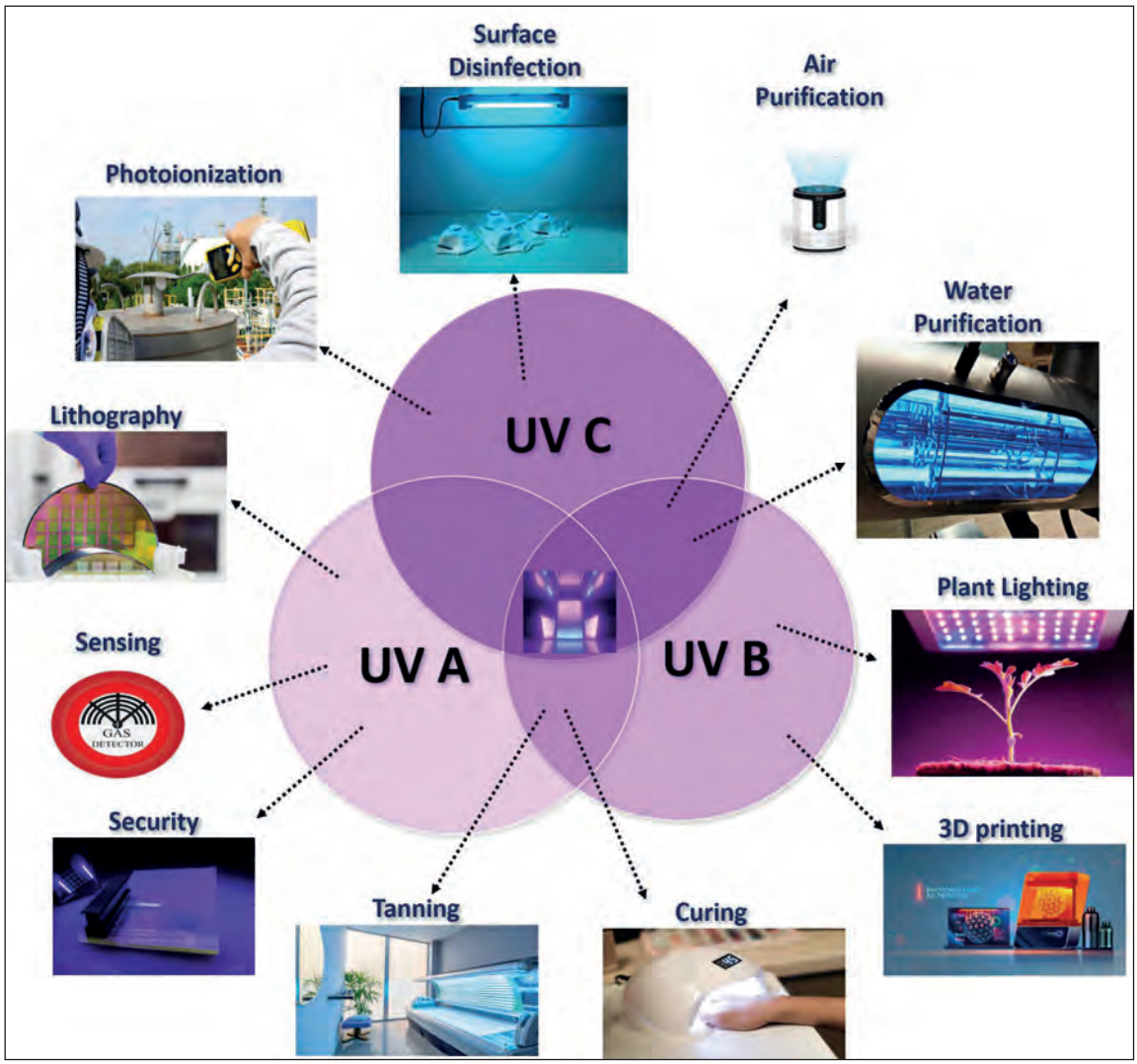

Figure 1. Applications of light-emitters in the UV. Radiation is generally divided into three spectral bands, based on specific wavelengths: UVA (400 nm-320 nm), UVB (320 nm-280 nm), and UVC (280 nm-100 nm).

to solicit photochemical reactions in living organisms; and they provide an option for treating several skin diseases, such as psoriasis, vitiligo, and cutaneous T-cell lymphoma.

The traditional sources of UV lamps contain either mercury, xenon, argon, deuterium, or an excimer. All are unsatisfactory on many fronts, being bulky, fragile, expensive, low in efficiency, limited in life span, toxic in nature, and only capable of emitting at a few specific wavelengths. A far better alternative is the UV LED, which combines compactness with a nontoxic material composition, a lower power consumption, a quick response time, a long lifetime, and tuneable emission across the entire UV region.

Thanks to these strengths, market analysts expect sales of the UV LED to climb in the coming years. Yole Développement predicts global revenue to increase from $320 million in 2020 to $1 billion in 2023, while Allied Market Research forecasts a compound annual growth rate of 21 percent over the next few years that will propel the value of this market to $1.7 billion by 2027.

Yet despite all this promise and expectation, the UV LED has its faults. Chief amongst them is a low efficiency, which plummets as the emission wavelength heads deeper into the UV. The efficiencies of these AlGaN-based devices are in single digits, held back by a number of factors that include a high density of dislocations, induced polarization fields, electron leakage, poor *p*-type doping, inefficient hole transportation, substantial internal absorption, a high internal total reflection, and a dominant transverse magnetic mode that drags down the light extraction efficiency. Despite much effort to improve both the internal quantum efficiency and the light extraction efficiency, the external quantum efficiency – the product of those two factors – is still low in planar AlGaN UV LEDs.

Recently, UV LEDs formed from AlGaN nanowires have emerged as a promising candidate for addressing some of the limitations of their planar counterparts. Merits of the nanowire LED include a near-absence of dislocations and a reduced piezoelectric polarization, thanks to effective strain relaxation. Additional merits of the nanowire structures

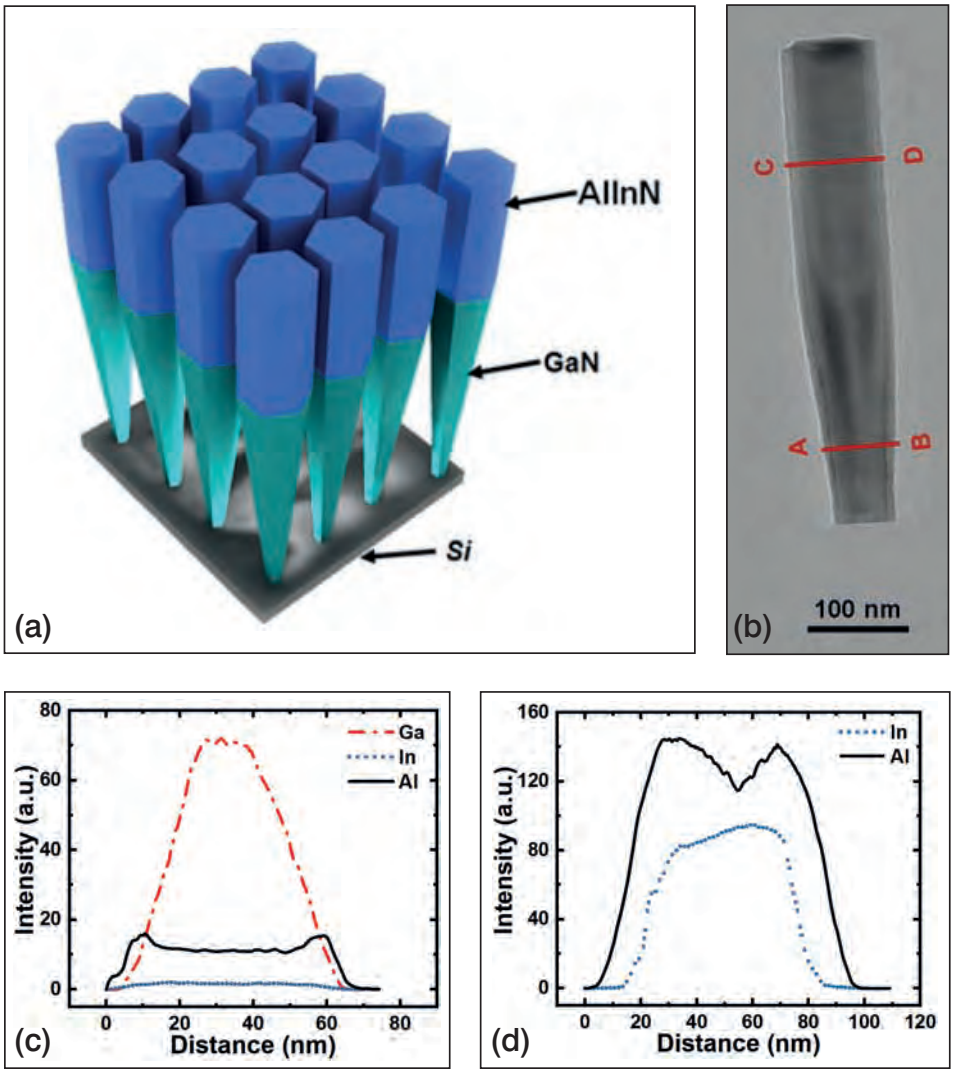

Figure 2. (a) AlInN/GaN nanowires can be grown on silicon substrates. (b) A transmission electron microscopy image of the AlInN/GaN nanowire, clearly showing the presence of a core-shell structure. Energy dispersive X-ray spectrometry line scan profile showing (c) the quantitative variation in gallium, indium and aluminium signals along lines A-B, and (d) variation in the indium and aluminium signal along lines C-D (Adopted from R. T. Velpula *et al*. Sci. Rep. **10** 2547 (2020)).

are the realisation of efficient *p*-type doping, effective thermal dissipation, and a high light-extraction efficiency. However, there is still much work to do – while the performance of the AlGaN nanowire UV LED has improved, its external quantum efficiency is still below 1 percent at deeper wavelengths, and higher values are needed before this device can be deployed in practical applications.

AlGaN or AlInN

One promising pathway to improving the performance of the UV LED is to switch from AlGaN nanowires to those made from AlInN. The latter is relatively unexplored, but holds great potential for UV and visible LEDs. Strengths of this ternary include lattice-matching to GaN with an indium content for AlInN of around 17-18 percent, and a high refractive index contrast with GaN.

In addition, AlInN compounds can be grown on both GaN and AlN templates – note that AlGaN is inimical to grow on GaN templates – and compared to AlGaN, AlInN offers wider windows of optimal alloy composition, especially in the deep UV.

Despite these tremendous advantages, progress with AlInN has been slow. Hampering efforts has been the immature epitaxial growth of high-quality AlInN. When grown by MBE, there tends to be significant compositional inhomogeneity, probably rooted in the extremely large differences in the optimal growth temperatures of the two 'components' – for InN, growth should take place at around 450 °C, while for AlN it needs to be in the region of 800 °C.

The solution is to grow AlInN nanowires under nitrogen-rich conditions, while dialing back the aluminium flux. This yields high-quality AlInN nanowires that are free from compositional inhomogeneities found in the AlInN layers. Adopting this approach is our team at the New Jersey Institute of Technology, which has pioneered the world's first axial AlInN nanowire-based UV LEDs.

We have produced our vertically aligned, self-organized AlInN/GaN core-shell nanowires on *n*-type silicon (111) substrates using an RF plasma-assisted Veeco Gen II MBE tool (see Figure 2 (a)). Epitaxial conditions for our GaN nanowires include

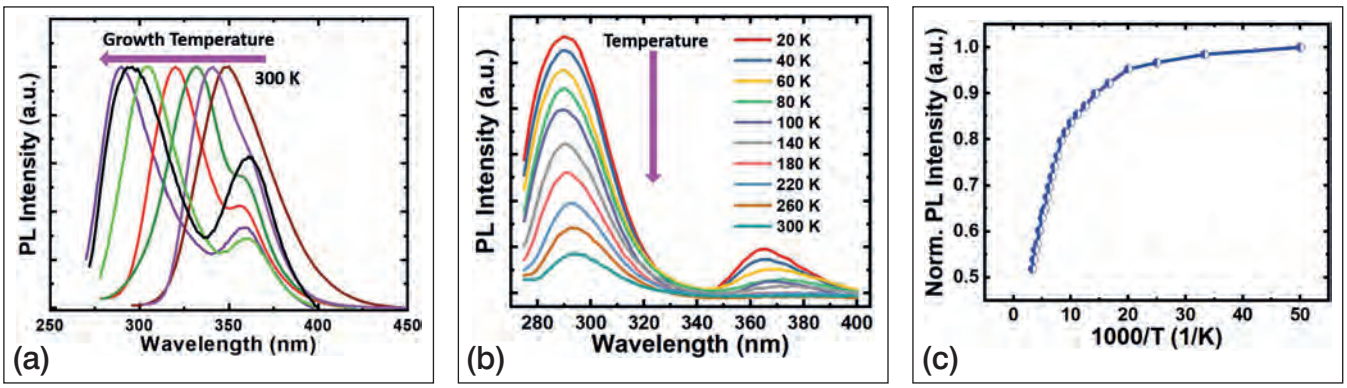

Figure 3. (a) Photoluminescence spectra of AlInN/GaN nanowires. Peak emission varies from 290 nm to 355 nm. (b) Temperature-dependent photoluminescence intensity of AlInN/GaN nanowires measured from 20 K to 300 K. (c) Photoluminescence intensities of AlInN/GaN nanowires under different temperature conditions (adopted from R. T. Velpula *et al*. Sci. Rep. **10** 2547 (2020)).

a growth temperature of 770 °C, a nitrogen flow rate of 1.0 sccm, a forward plasma power of 400 W, and a gallium beam equivalent pressure of 6 × 10^{-8} Torr. After growth of the GaN nanowires, we add self-organized AlInN segments that provide UV light emission. By varying the indium and aluminium beam flux and/or the substrate temperature, we control the composition of the active region.

Scanning transmission electron microscopy has enabled the characterisation of the structural properties of our AlInN/GaN nanowires. This technique uncovers the presence of GaN and AlInN segments (see Figures 2(b)-(d)) and reveals that the wire diameter increased from the GaN segment to the AlInN portion and remained constant on the top of the nanowire. Our images also suggest that a core-shell AlInN/GaN structure spontaneously formed during epitaxial growth of the AlInN layer. If that's the case, this is an asset, because a core-shell structure offers strong carrier confinement and reduced non-radiative recombination on the nanowire surface, leading to enhanced optical characteristics.

We turned to photoluminescence to investigate the optical properties of our portfolio of AlInN/GaN nanowires. This involved pumping our AlInN/GaN nanowire structures, fabricated under different growth conditions, with a Kimmon Koha 266 nm laser. Resulting spectra (see Figure 3 (a)) feature a peak emission at around 368 nm, related to emission from the GaN nanowire template, and another peak between 290 nm and 355 nm, with a position that depends on the growth temperature, which alters the aluminium composition in the AlInN layers.

A more thorough investigation has been undertaken for AlInN nanowires produced with a growth temperature of 710 °C. These wires have a strong emission at 295 nm, with an associated spectral linewidth of 28 nm. Using 10 mW excitation, we have measured the photoluminescence at a variety

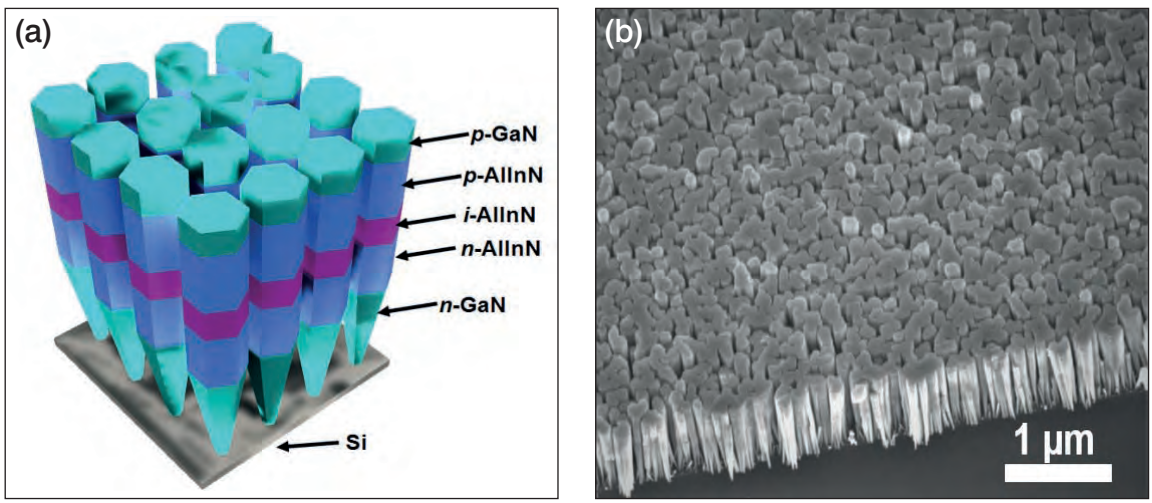

Figure 4. (a) A silicon substrate provides a platform for a *p-i-n* AlInN nanowire LED structure. The devices contain a layer of GaN:Si that is about 200 nm-thick, as well as 100 nm $Al_xIn_{1-x}N$:Si/40 nm *i*-$Al_yIn_{1-y}N$/100 nm $Al_xIn_{1-x}N$:Mg, and 10 nm GaN:Mg (b) 45o tilted scanning electron microscopy image of p-i-n AlInN nanowire LED sample (adapted from R. T. Velpula *et al*. Sci. Rep. **10** 2547 (2020)).

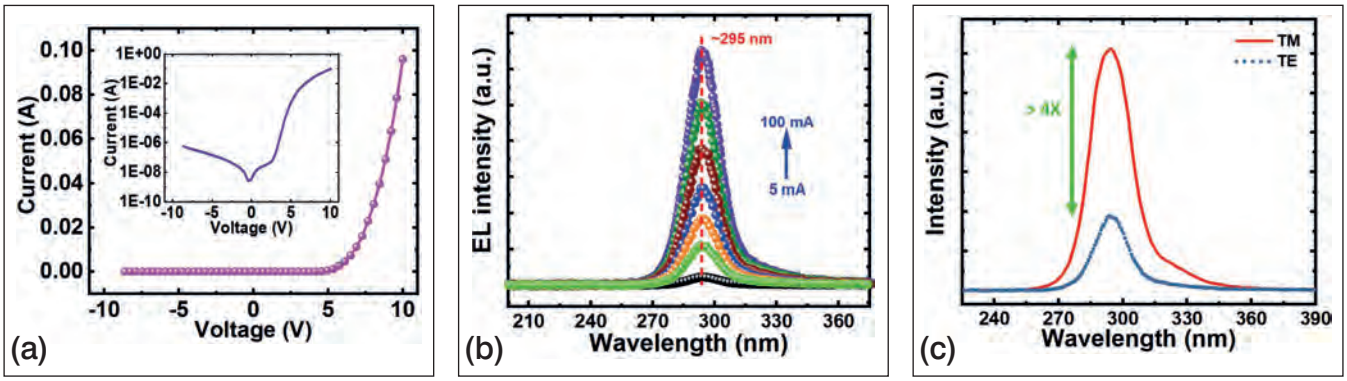

Figure 5. (a) Current-voltage characteristics of the AlInN UV nanowire LED. The inset shows the current-voltage plot for the AlInN UV LED on a semi-log scale. (b) Electroluminescence spectra of the AlInN UV nanowire LED. (c) The transverse-magnetic (solid line) and transverse-electric (dotted line) polarized spectra of the AlInN UV nanowire (adopted from R. T. Velpula *et al*. Sci. Rep. **10** 2547 (2020)).

of temperatures between 20 K and 300 K (see Figure 3(b)). This provided an estimate of the internal quantum efficiency, calculated by comparing the integrated photoluminescence intensities of emission from the AlInN layer at room temperature and at 20 K, and assuming that the internal quantum efficiency at 20 K is close to unity. This approach suggests that the room-temperature internal quantum efficiency of the AlInN/GaN nanowires is 52 percent (see Figure 3 (c)). We attribute this relatively high value to the strong carrier confinement provided by the AlInN shell and the nearly intrinsic AlInN core.

We have fabricated nanowire LEDs based on this active region and featuring a *p-i-n* structure (see Figure 4(a) for details). Scanning electron microscopy of these AlInN nanowire LEDs reveals that the diameter at the top of the nanowire is typically 90 nm, a suitable dimension for device fabrication (see Figure 4(b)).

Fabrication of our devices begins by cleaning the epiwafers in HCl and then HF. These steps remove the oxide layer from the backside of the silicon substrates and native oxides from the nanowire surface. We then create a *n*-contact on the backside of the silicon by depositing a metal stack, comprising 20 nm of titanium and 120 nm of gold; and turn to electron-beam evaporation to create a *p*-metal contact by depositing 10 nm of nickel and 10 nm of gold. After this, we add 20 nm of nickel and 120 nm of gold, on top of the device, to serve as a metal pad. We anneal the resulting structure at around 550 °C for 1 minute to achieve low contact resistance.

Our AlInN LEDs exhibit excellent current-voltage characteristics, combining a low resistance at room temperature with a turn-on voltage of about 5 V, a value that is at least as good as that of AlGaN UV LEDs operating in this spectral domain (see Figure 5 (a)). These devices produce strong UV light emission at around 295 nm at injection currents from 5 mA to 100 mA (see Figure 5 (b)).

The particular polarization of the light generated within the UV LEDs can govern the output of this device. Using a 10 A cm^{-2} injection current, we have investigated the polarization of our devices, defining the transverse-magnetic and transverse-electric directions as those with electric fields parallel and perpendicular to the *c*-axis, respectively. These measurements reveal that the light emission in our devices is predominantly transverse-magnetic polarized – this signal is more than four times that of

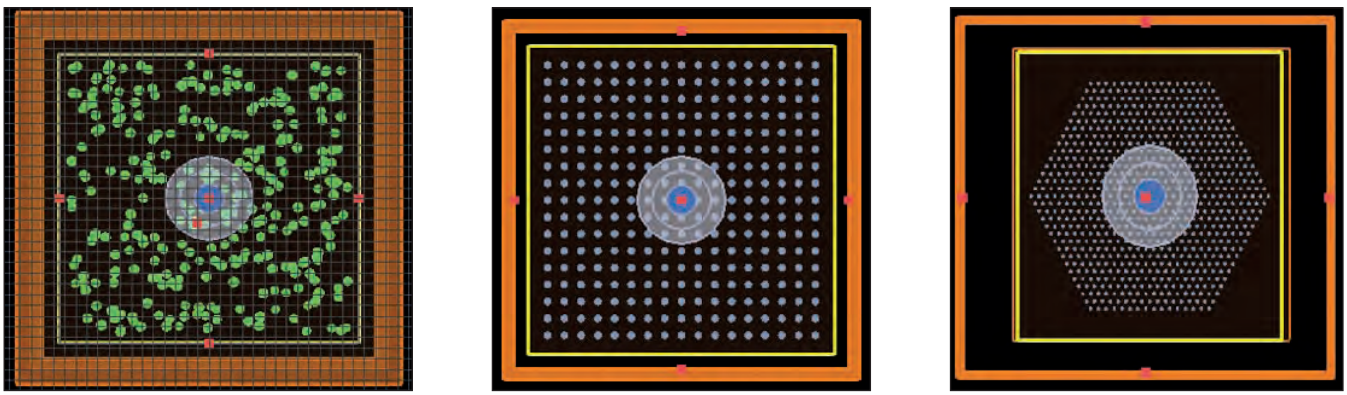

Figure 6. Top view of random array (left), square array (middle), and hexagonal array (right) of AlInN nanowire UV LEDs (adopted from B. Jain *et al*. Opt. Exp. **28** 22908 (2020)).

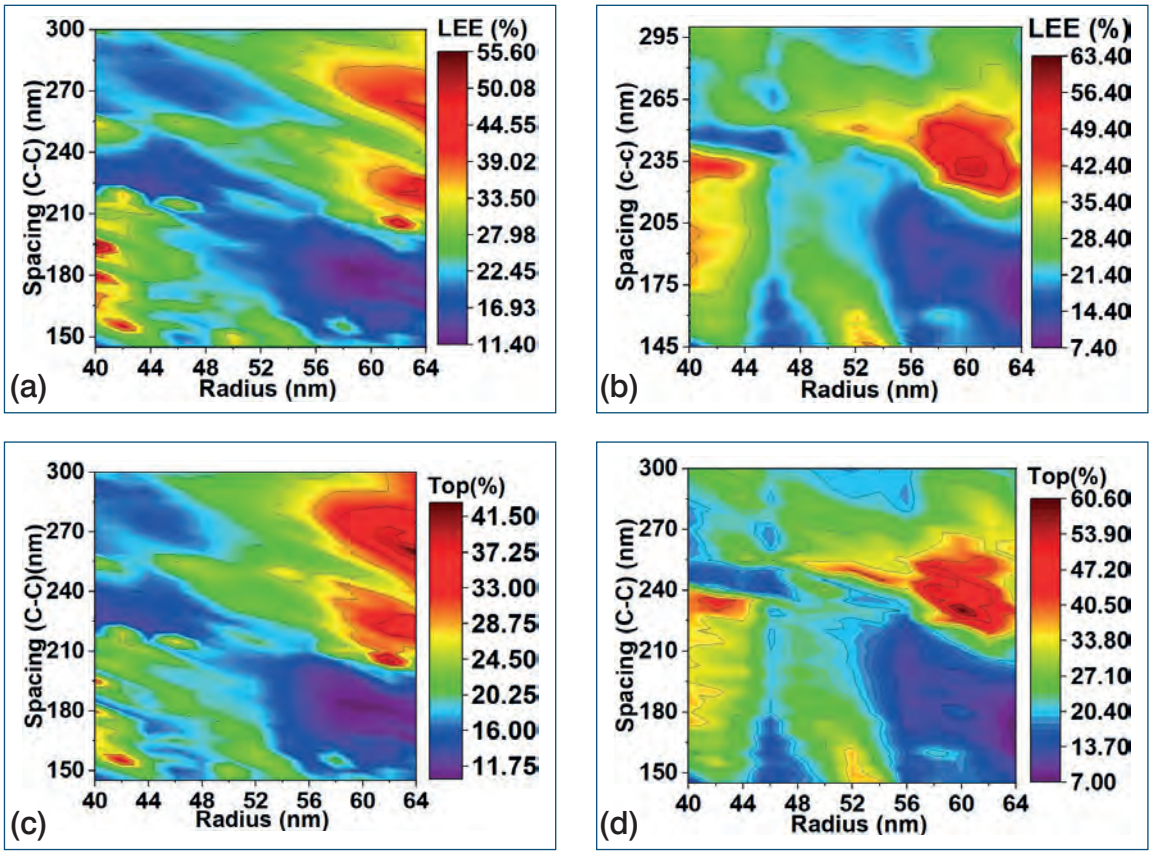

Figure 7. Contour plot of the light-extraction efficiency for a differing nanowire radius and spacing for a square array (a) and a hexagonal array (b) of AlInN nanowire UV LEDs. Contour plot of the light-extraction efficiency from the top, for a differing nanowire radius and spacing for the (c) square array and (d) hexagonal array of AlInN nanowire UV LEDs (adopted from B. Jain *et al*. Opt. Exp. **28** 22908 (2020)).

the transverse-electric mode (see Figure 5 (c)). To enhance light extraction through optimisation of polarization, we have considered the morphology of our devices. This theoretical study considered photonic crystal structures with randomly grown, square, and hexagonal lattices (see Figure 6).

The benchmark for this work is the randomly distributed nanowire array, which has an average light-extraction efficiency between 20 percent and 35 percent. To increase this, we investigated square and hexagonal arrays with varying nanowire radii and lattice spacings (see Figure 7 (a) and (b) for contour plots of the light extraction efficiency as a function of nanowire radius and spacing for both topologies).

Our calculations show that the maximum light-extraction efficiency for the square array is 56 percent, realised with a spacing of 195 nm and a radius of 40 nm. Better results are possible with hexagonal nanowires, with light extraction efficiency hitting 63 percent for a spacing of 230 nm and a radius of 60 nm. These results underscore the critical role that geometry plays in directing the generated photons from the active region to air.

Optimising polarization is behind these high values. While square and hexagonal arrangements support vertical light emission, these nanowire structures favour highly transverse-magnetic-polarized emission (see Figures 7 (c) and (d)). For hexagonal array nanowires, of the 63 percent light extraction efficiency, 60.6 percent of this comes through the top surface, a very encouraging result when considering practical applications.

Our work, involving the introduction of the world's first axial AlInN core-shell nanowire UV LEDs, offers a new pathway for producing sources in this spectral range. Devices are in their infancy, and performance is sure to improve through optimising the LED structure, nanowire morphology, diameter and spacing. They are long-term goals for us, but our efforts will initially head in a different direction, reducing emission wavelengths to below 230 nm, so that these LEDs can serve in air and surface disinfection.

Further reading

R. T. Velpula *et al*. Scientific Reports **10** 2547 (2020)

B. Jain *et al*. Opt. Exp. **28** 22908 (2020)

R. T. Velpula *et al*. Optical Materials Express **10** 472 (2020)

R. T. Velpula *et al*. CLEO: Science and Innovations (pp. STu3P-4). Optical Society of America, 2020.

Switching to silicon substrates for satellite communication

Today's solid-state high-power power amplifiers operating in the microwave domain are based on the GaN-on-SiC HEMT. Replace the SiC with silicon and key attributes remain, while costs fall, thanks to production on larger wafers

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BROADBAND ACCESS SERVICES are destined for unprecedented growth this decade. As 5G is rolled out, data rates are climbing to 100 Gbit/s, while, in urban areas, simultaneous connections will total more than a million for every square kilometre. Alongside traditional services, such as video streaming, audio calls and data sharing, billions of daily used objects will be hooked up to the internet, including washing machines, fridges and ovens.

To underpin this new era in connectivity, there will need to be a new paradigm for the underlying network. This will include: a higher cell density, and thus a lower peak power; the introduction of a carrier frequency in the K-bands (18-27 GHz); an extended bandwidth; alternative channel access techniques, such as beam-division multiple access (BDMA); massive MIMO; and the use of more efficient spectrum aggregation signals. But even with all of this innovation, this network, which relies upon terrestrial infrastructures, will still fail to satisfy all of tomorrow's requirements.

One option for addressing this issue is to combine terrestrial infrastructure with satellite communication. Such a move will provide a major growth opportunity for geostationary earth orbit very-high-throughput satellites. These satellites can realise phenomenal data rates of more than 1 Tbit/s, while increasing the flexibility of the overall network, by allocating capacity where it is needed.

A key step in the deployment of very-high-throughput satellites is the development of high-performing space-borne equipment operating at high frequencies. It is envisaged that the feeder link, which is the radio channel between the satellite and a ground station, will be in the Q/V bands, so typically 40 GHz. Meanwhile the data link, providing the radio channel between the satellite and the end users, will reside in the K_a-band, at a frequency of 18.75 GHz.

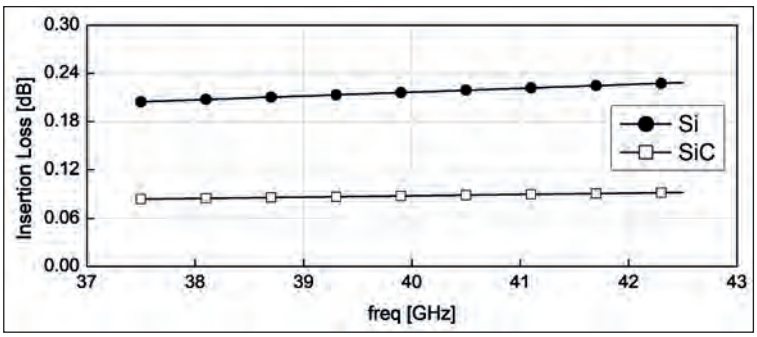

Figure 1. Simulated insertion loss of a transmission line with a Z_0= 50 Ω characteristic impedance and 1 mm length realized on silicon (filled symbols) and SiC (empty symbols) substrates.

Very-high-throughput satellites feature many beams. To accommodate this, satellites must house more equipment, realized ideally through miniaturization. New hardware needs to be lighter and smaller, as well as more reliable and better at thermal management.

Fulfilling all these requirements at the spacecraft level hinges on increasing the performance of the power amplifier, which sits at the last stage of the transmitting channel. This sub-unit of a payload consumes more than 75 percent of the overall DC power, so governs systems efficiency and thermal management

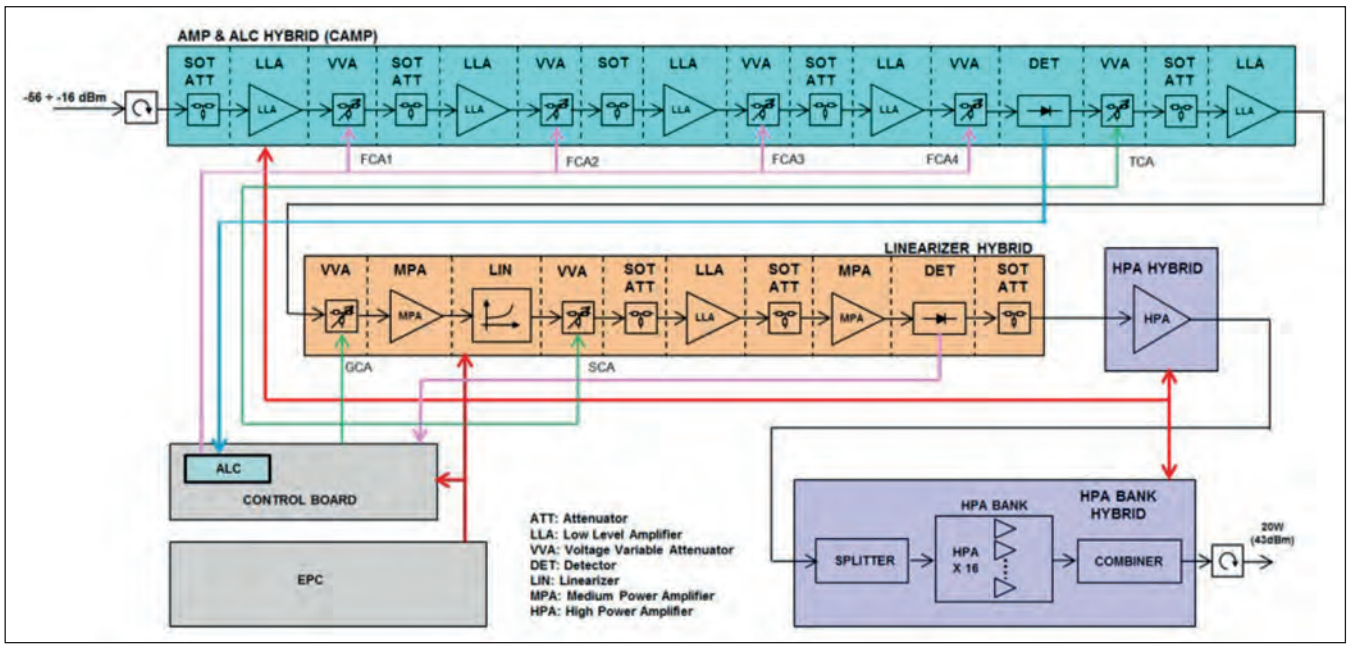

Figure 2. RF line-up of the solid-state power amplifier. It is composed by four sub-units, namely a Channel Amplifier (CAMP Hybrid), Linearizer Hybrid, HPA Hybrid and HPA Bank.

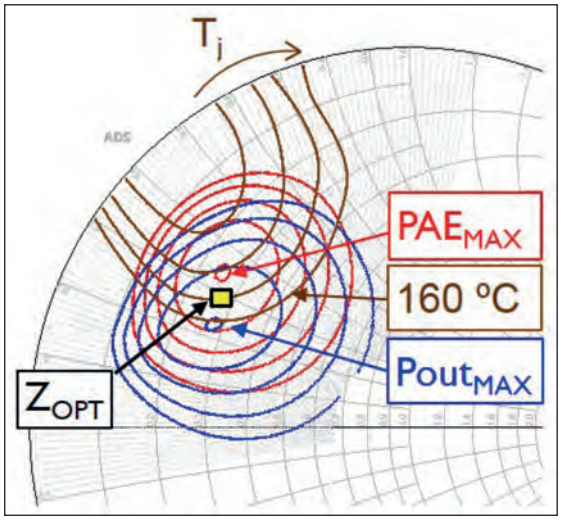

Figure 3. Simulated load-pull counters of the 4 x 75 μm device at a frequency of 40 GHz. Output power (blue), PAE (red), junction temperature (brown) and selected impedance (yellow).

requirements, while also impacting the reliability, mass and volume of the transmitter. In addition, the power amplifier determines the output power level and the spectral regrowth of the transmitted signal – these traits are determined by linearity and power characteristics.

Historically, when designers of communication satellites have needed power at high frequencies, they have turned to travelling-wave tube amplifiers. Their choice has been limited, because solid-state power amplifiers have fallen short of the performance required. But this has changed with the introduction of GaN, which has propelled solid-state technology to new levels of efficiency and power density, as well as a higher operating voltage and a higher impedance, which eases matching.

There are currently two types of process for producing GaN RF devices: one is for SiC substrates, and the other for silicon. The former has proven to be the best foundation for making high-power, efficient PAs at microwave frequencies, such as the K_u-band. However, silicon has much promise. This platform can exploit key features of most common GaN-on-SiC technologies, while drawing on additional benefits, including a reduced production cost, driven by larger wafers.

GaN-on-silicon: Concerns...

At this stage, doubts surround the suitability of GaN-on-silicon HEMTs for satellite communication. While studies have proven that GaN-on-SiC power amplifiers are a worthy replacement for tubes for several applications, the prospects for the GaN-on-silicon amplifier are held back by concerns related to thermal management and passive structure losses.

There is good reason to question the thermal management of the GaN-on-silicon HEMT, given that the thermal resistance of this material system is roughly double that of its GaN-on-SiC counterpart, due to the inferior thermal conductivity of the substrate. Regardless of the substrate type, the junction temperature of a GaN device is limited to ensure reliability in space – the European Space Agency insists that it does not exceed 160 °C. Due to this constraint, the dissipated power density for GaN-on-silicon technology can only be half of that for its SiC counterpart, and for equivalent devices, RF power density is also halved.

To illustrate this, consider two 4 x 75 μm technologies, differing only in the substrate type (they have the same bias voltages, gain, power density, efficiency and so on). The GaN-SiC device produces an RF output power of 1.5 W, equating to a power density of 5 W/mm. The associated power-added efficiency is 50 percent, and the gain 10 dB. The performance is realised at a junction temperature below 160 °C, by restricting the base plate to 80 °C, conditions that lead to a power dissipation of 4.5 W/mm.

In comparison, the equivalent silicon device, having the same power-added efficiency, gain and periphery, has to operate at half the power density and power dissipation to ensure a junction temperature below

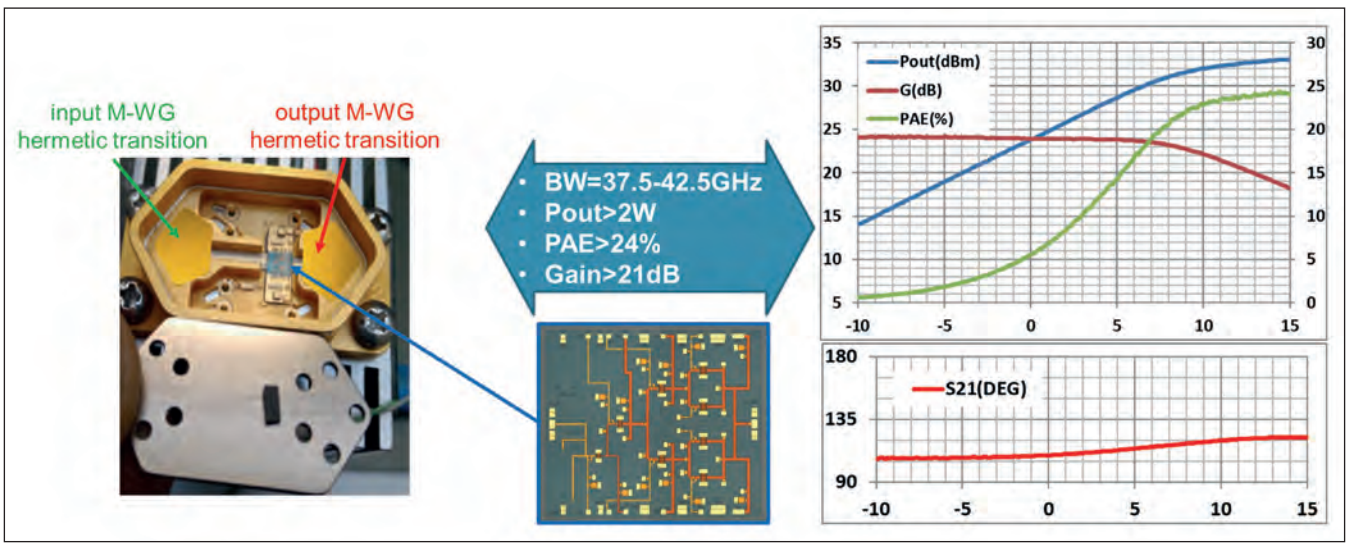

Figure 4. The assembled MMIC provides good performance at 40 GHz.

160 °C. To fulfil this requirement, the power density is limited to 2.5 W/mm, while power dissipation is around 2.25 W/mm.

Concerns related to losses in passive structures made from GaN-on-silicon are focused on the transmission lines. Simulations suggest that the insertion loss of a 1 mm length 50 Ω transmission line in the Q-band is 0.13 dB higher for GaN-on-silicon than it is for GaN-on-SiC (see Figure 1). This insight shows that when designing an amplifier with GaN-on-silicon technology, it is better to synthesize matching networks using lumped elements than distributed ones.

...and strengths

There are some remarkable advantages associated with GaN-on-silicon, including a lower material cost and access to larger wafers, which are well-suited to production volumes for 5G. By producing amplifiers from GaN-on-silicon, risks of import/export restrictions are diminished, making it easier to procure material.

And last but by no means least, GaN-on-silicon is compatible with heterogeneous integration in SiGe/CMOS technologies, so it offers many opportunities for making highly integrated, multi-functional chips. To help drive adoption of the GaN-on-silicon power amplifiers in tomorrow's communication satellites, our Italian collaboration – a partnership between researchers at the University of Rome 'Tor Vergata' and Thales – has built and characterised a Q-band GaN-on-silicon power amplifier. It features an RF tray, formed using a waveguide structure to combine sixteen MMIC power amplifiers realised with a commercial 100 nm gate length GaN-on-silicon process.

Despite the inherent drawbacks of the GaN-on-silicon HEMT, our power amplifier produces more than 20 W, has a noise-to-power ratio exceeding 18 dB, and operates at a power-added efficiency in excess of 15 percent. Shown in Figure 2 is the RF line-up of this amplifier, which delivers a level of performance that showcases the outstanding potential of GaN-on-silicon technology for space applications.

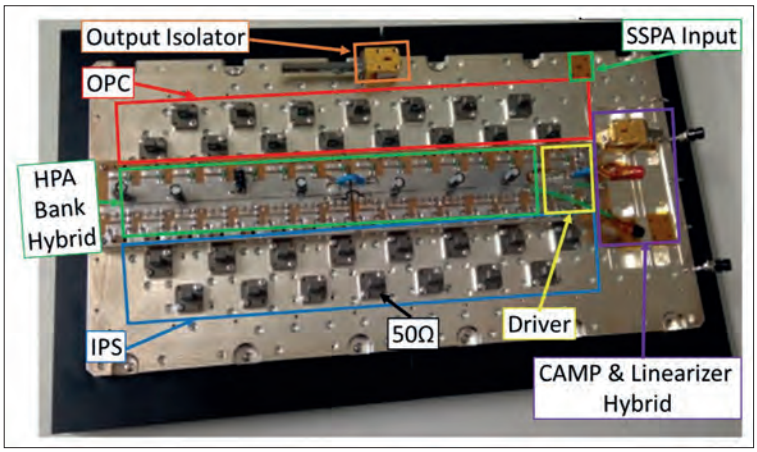

Figure 5. The splitter/combiner structures delivers an encouraging performance from 35 GHz to 45 GHz.

The first part of our power amplifier is the channel amplifier that provides an output of around -3 dBm. This sub-unit has a cascade of several low-level amplifiers and variable/fixed attenuators, carefully chosen to control the uplink flux, which can be adjusted by either ground telecommands – a fixed gain mode – or by an automatic level control loop. The latter is capable of compensating for in-orbit ageing of power amplifier gain, using a feedback signal provided by an integrated detector.

Downstream of the channel amplifier is a linearizer, primarily there to compensate for the nonlinearity of the high-power-amplifier bank that follows. The linearizer is designed to provide, as much as possible, equal but opposite amplitude-to-amplitude and amplitude-to-phase distortions with respect to those experienced by the high-power-amplifier bank.

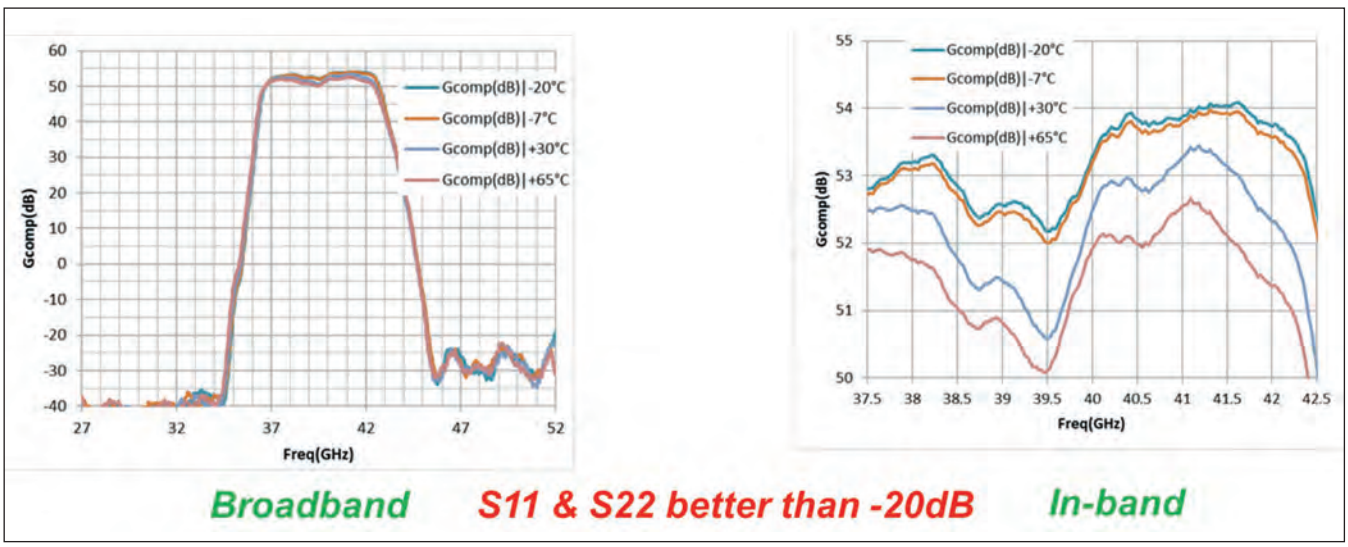

Figure 6. Measured small-signal performances of the solid-state power amplifier.

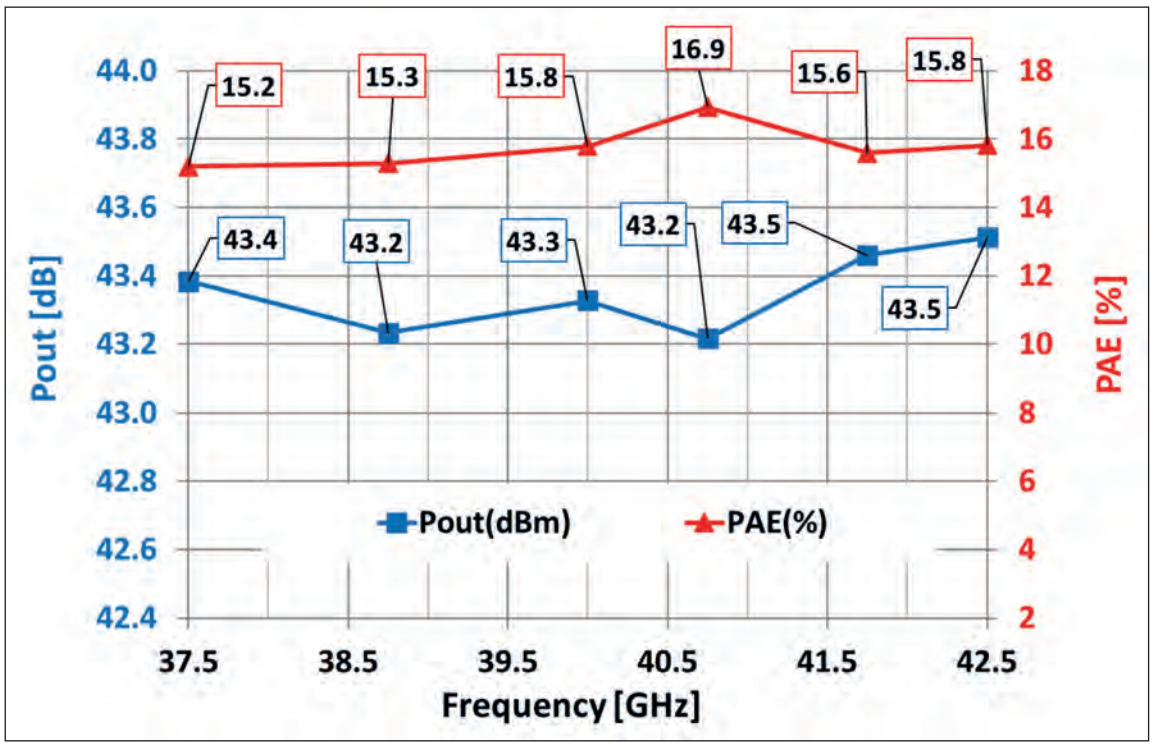

Figure 7. Measured large-signal performances of the solid-state power amplifier.

Controlling the overlap between the expansion of the linearizer and the compression of the high-power-amplifier bank is a setpoint control attenuator. In this arrangement, the linearizer compensates for up to 7 dB of gain compression and +/- 45° of phase variation, and provides a constant output power of 7 dBm.

The signal from the linearizer is fed to the high-power-amplifier hybrid, which drives, in a 1-to-16 ratio, the high-power-amplifier bank. The last two sub-units are implemented in an WR-22 waveguide, and exploit the MMIC PA developed ad-hoc on a commercial 100 nm gate length GaN-on-silicon process available at the Ommic foundry.

During the development of our MMIC, we devoted much effort to accounting for the thermal, electrical and physical constraints of GaN-on-silicon technology. This included undertaking a series of load-source pull simulations on devices with a different geometry, evaluated using the centre frequency, which is 40 GHz. For each geometry, as well as calculating the output power, power-added efficiency and gain, we considered the resulting junction temperature. For this work we assumed a base plate temperature of 80 °C, which corresponds to the maximum value expected below the MMIC.

For our load-pull simulations, we selected the optimum load impedance for the 4 x 75 μm device (the values for the output power, power-added efficiency, and junction temperature are shown in Figure 3). To ensure that we comply with the de-rating rules while maximizing the output power, we have selected a load impedance that is between those for maximum power and power-added efficiency, and we produce a junction temperature contour that is slightly lower than 160 °C. By adopting these conditions, we give ourselves a margin when implementing our actual MMIC. Although this choice sacrifices efficiency performance by about 1 percent, it guarantees fulfilment of the power level requirement at the circuit level.

Drawing on the results of our load-source pull simulations, we have undertaken a power budget analysis. Insights provided by this led us to design a MMIC based on a four-stage corporate architecture, with a final stage comprising four 4 x 75 μm devices driven by the same device in a 1:2 ratio. For the second and first stage, we used a single 8 x 50 μm and a single 2 x 50 μm device, respectively.

All of the MMICs used to form our power amplifier are equipped with an input and output microstrip-to-waveguide hermetic transition. This is visible in the picture of our MMIC, shown in Figure 4 alongside plots illustrating typical performance from 37.5 GHz to 42.5 GHz. Output exceeds 2 W, while the associated efficiency and gain are greater than 24 percent and 21 dB, respectively.

We have connected sixteen MMICs in the high-power-amplifier bank using a WR-22 waveguide splitter/combiner network. In our design there are fifteen T-magic structures, with a response that has been carefully optimised to minimize losses while ensuring a matching better than 20 dB at all ports. A waveguide isolator is added at the output side to improve the

matching of the high-power-amplifier bank. We have measured losses for both the splitter and the combiner of 0.8 dB, and 0.3 dB for the isolator, giving a loss for the network of 1.9 dB.

Our power amplifier, including the WR-22 waveguide input and output isolators, weighs 5.5 kg and has dimensions of 45 cm by 22 cm by 7.2 cm (a picture is shown in Figure 5). This unit is powered by two positive voltages – 3.5 V, provided by GaAs devices, and 11.25 V, produced by GaN devices – and has a single bias voltage of -8.0 V, conditioned for the gates. For space applications, the thermal design of the amplifier is of upmost importance.

It is critical that the junction temperature of any active device does not exceed a safe figure for that particular technology, in order to guarantee reliable operation over the satellite lifetime, typically 15 years. For our amplifier, accurate thermal and mechanical design ensures that the hottest GaN-on-silicon MMIC never exceeds 160 °C, so long as the base plate temperature is no more than 65 °C.

Measurements of small-signal performance of our amplifier for base plate temperatures ranging from -20 °C to +65 °C, when the automatic level control loop is active, show that the forward voltage exceeds 53 dB, with a ripple lower than +/- 1dB in the overall operating bandwidth of 37.5 GHz to 42.5 GHz (see Figure 6). Input and output return losses are better than 20 dB, and gain variation over temperature is limited to less than 2 dB over 85 °C.

We have also measured our amplifier's performance for a fixed gain of 65 dB at a base plate temperature of 65 °C. Saturated output power exceeds 20 W, with a power-added efficiency exceeding 15 percent, aided by a DC-DC converter efficiency of 90 percent (see Figure 7). Overall power consumption is 155 W at saturation, falling to 100 W for a 3 dB back-off, corresponding to a 10 W RF output power. Alongside efficiency, the linearity of a power amplifier is of paramount importance.

Linearity is critical in applications that include very-high-throughput satellites, which involve the use of time-varying envelope signals that feature a significant peak-to-average power ratio. We evaluate our linearity by measuring the noise-to-power ratio. This figure-of-merit, determined by driving our amplifier with hundreds of uncorrelated carriers, is 18 dBc (average) at an output power of +43 dBm (see Figure 8).

Our results compare well with other solid-state power-amplifiers, and highlight that GaN-on-silicon technology, despite its differences to GaN-on-SiC, can still yield high-performing power amplifiers in the Q-band for serving space applications.

Despite trailing travelling-wave tube amplifiers in efficiency – for the same power levels, they can hit 20 percent – our GaN-on-silicon-based design has a great deal to offer, combining a lower cost with graceful degradation and selectable form factor. The upshot is a significant benefit for satellite designers.

The authors wish to acknowledge the Italian Space Agency (ASI) for funding this work in the context of project KALOS-DEVAQ within ESA's ARTES C&G Technology Program. Particular thanks are due to Francois Deborgies from ESA/ESTEC for his expertise and technical support.

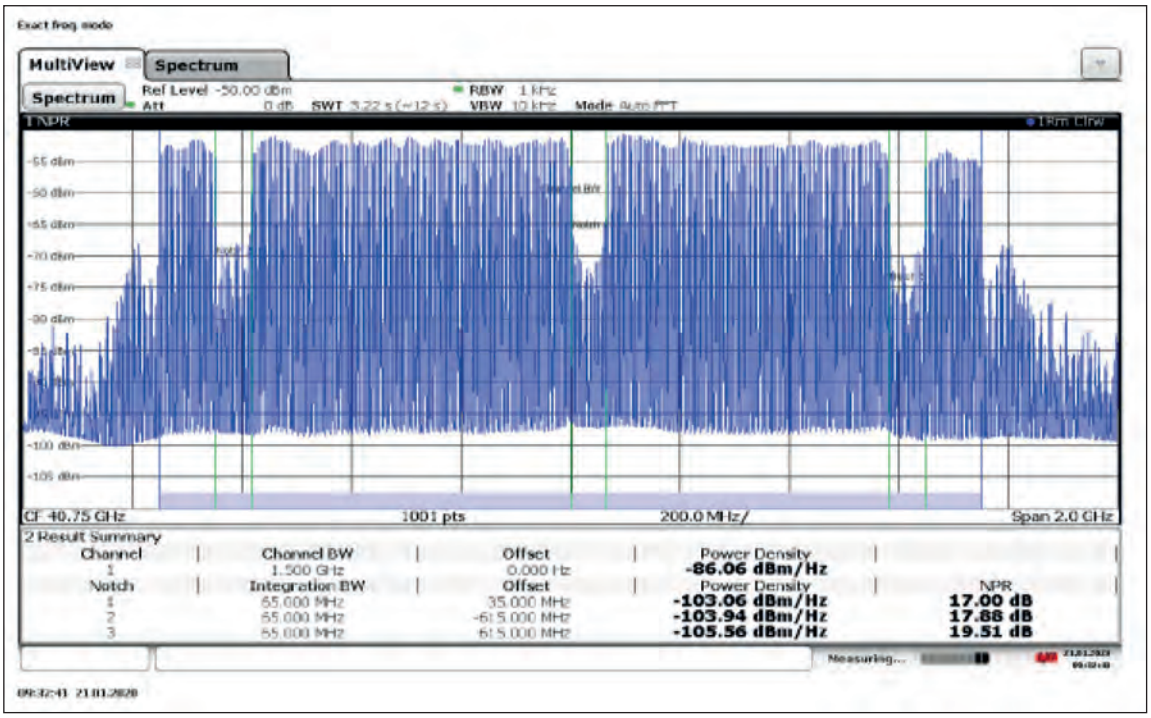

Figure 8. Measured noise-to-power (NPR) of the solid-state power amplifier (SSPA). This measurement was made by driving the SSPA with 301 uncorrelated carriers occupying a frequency band of 1.5 GHz large and applying three notches 65 MHz large.

InP empowers phased-array radar

Delivering record efficiencies in the Q-band, MMICs made from InP HBTs are the ideal choice for phased-array radar

BY ANDREA ARIAS-PURDUE, PETRA ROWELL, MIGUEL URTEAGA, KEISUKE SHINOHARA, ANDY CARTER AND JOSH BERGMAN FROM TELEDYNE SCIENTIFIC AND IMAGING AND KANG NING, MARK RODWELL AND JAMES BUCKWALTER FROM THE UNIVERSITY OF CALIFORNIA AT SANTA BARBARA

THE DEVELOPMENT of radar can be traced back as far as the late nineteenth century, to a time when German physicist Heinrich Hertz first demonstrated the reflection of radio waves by metallic objects. Exploiting this observation, engineers in the early twentieth century built a growing number of radar systems. While representing a staggering achievement, this traditional design has its downsides: it is bulky; and it takes time to re-orientate the direction of the beam, due to mechanical steering.

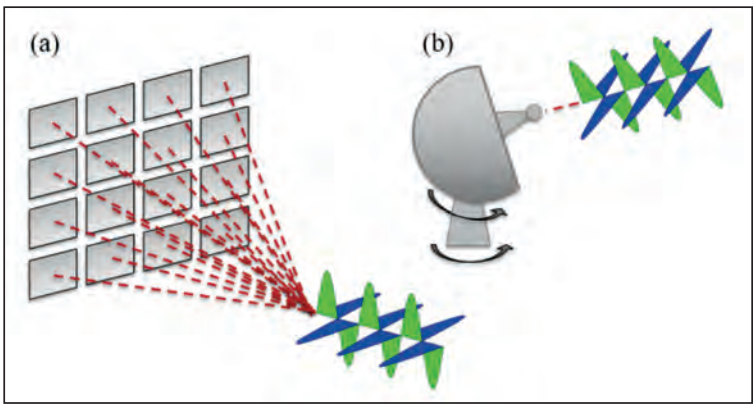

Figure 1. A 16-element phase-arrayed radar (a) and a conventional mechanically steered radar (b).

Addressing these weaknesses is the more recent phased-array radar, which features electronic synthesis of the beam. By adjusting the phase of the signal transmitted out of each element, it is possible to dial in the desired radiation pattern.

Lying at the heart of a phase-arrayed radar are full receiver and transmitter units, each equipped with an RF amplifier and antenna. First-generation units were constructed with silicon-based technology – more than a decade ago a team from Caltech broke new ground by demonstrating silicon-based phased array receivers with 8 elements, operating at 24 GHz.

However, more recently, due to demand for phased-array radar operating in the millimeter-wave – that is, above 30 GHz – new materials have been introduced, to cater for greater demands placed on the chip technology. As the frequency increases, the size of the chip must shrink, due to considerations associated with the element spacing due to the shorter wavelength of the radar technology. This leads to the need for a higher RF output power density per

unit chip, and a high efficiency that ensures a safe semiconductor device operating junction temperature and ultimately reliable operation.

The key to meeting all these criteria is to switch from using silicon-based devices to those based on III-Vs. At frequencies above 30 GHz, compound semiconductor devices are setting new benchmarks for: power density, judged in terms of Watts per chip area; raw power, measured in Watts; and efficiency for a given bandwidth. It is for this reason that our team from Teledyne Scientific and Imaging are developing phased-array technology based on InP HBTs, which we have used to make MMICs operating at 47 GHz with record power-added efficiency (PAE). We have selected this particular III-V because it has a high carrier mobility, and a higher bandgap than silicon and SiGe, attributes that enable high-voltage handling and a very high power gain at microwave frequencies – amongst the highest for any semiconductor system.

We produced our InP HBTs using our 0.25 μm process. The transistors that result have excellent RF figures-of-merit, including a cut-off frequency of around 350 GHz, a maximum oscillation frequency of 700 GHz, and an off-state collector-emitter breakdown voltage in excess of 4.5 V. For these devices, maximum available gain is 15-16 dB at 50 GHz, and output capacitance is just 1.87 fF/μm, easing tuning for transformation to a typical 50 Ω load (see Figure 2).

To evaluate the suitability of our InP technology for millimetre-wave power amplifiers, we have undertaken load-pull simulations. They involved simulating a single-stage amplifier, varying the load and source impedances, and, at each impedance pair, sweeping the RF input power and plotting the device response. Using this approach, we obtained values for output power, DC power, gain, and efficiency.

Our load-pull simulations indicate that our InP HBTs should produce an excellent peak PAE and associated RF output power across very wide bandwidths (see Figure 3). Note that the results that we report correspond to the fixed source and load impedance shown therein, which offered the best peak PAE across 24 GHz to 60 GHz, based on load and source-pull simulations. Great performance in this domain bodes well for millimetre-wave radar.

We have confirmed excellent power performance through load-pull measurements, performed on-wafer. Our use of a vector receiver-based load-pull system provides us with wave quantities at the input and output ports of the device. Measurements that we make include the reflected power at the input of the transistor. This enables accurate determination of both the device's power gain and its input reflection coefficient. We recorded values of a 57 percent PAE and an output power of 60 mW, when operating the device with a collector-emitter voltage of 2.8 V, an associated

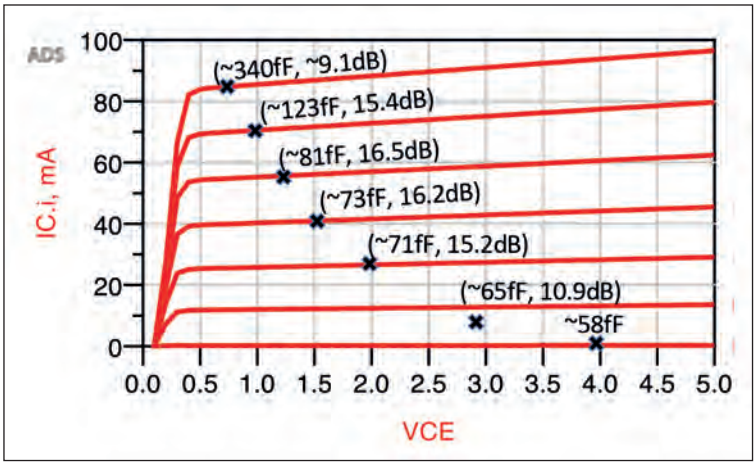

Figure 2. Simulated output current-voltage (I-V) curves of 10 μm² common emitter power cell, along with effective output capacitance and MAG at selected loadline bias.

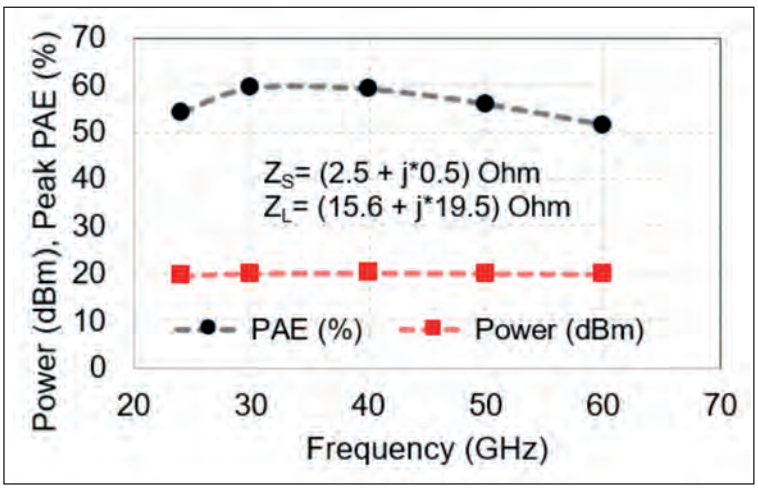

Figure 3. Load pull simulations results (power and PAE) at fixed source and load impedance of 20 dBm InP HBT power cell.

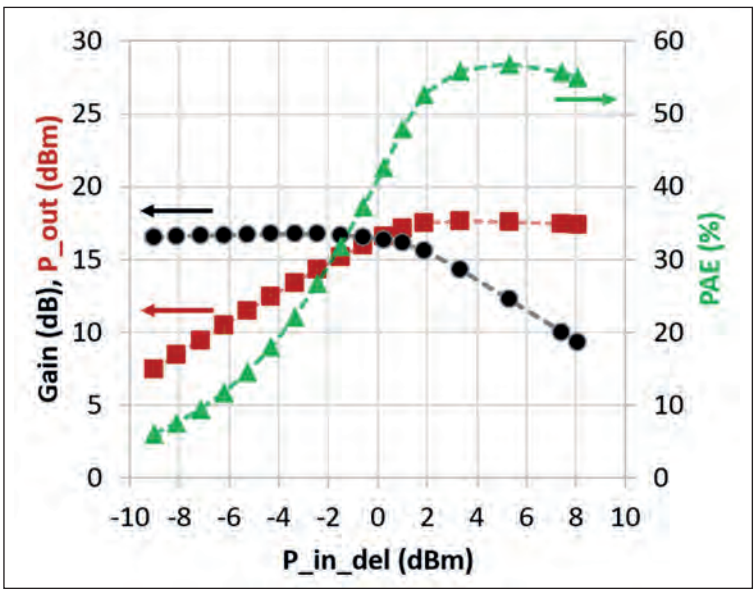

Figure 4. Load pull measurements of designed power cell (15 μm²). Measurements were made using an optimum gamma Γ_{LOAD} of 0.6 / 120°

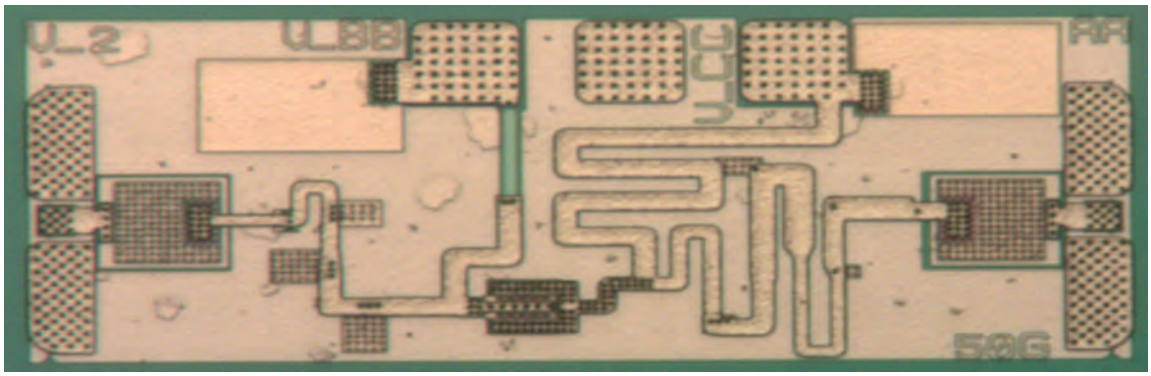

Figure 5. Micrograph of a fabricated InP HBT PA.

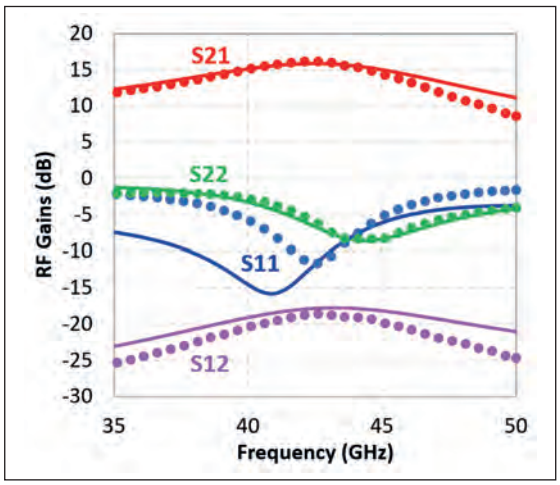

Figure 6. PA small signal response at V_{CC}= 2.75 V, V_{BB}=2.35 V ($I_{C,Q}$ = 47 mA). The solid lines correspond to simulated performance while the symbols correspond to the measured response.

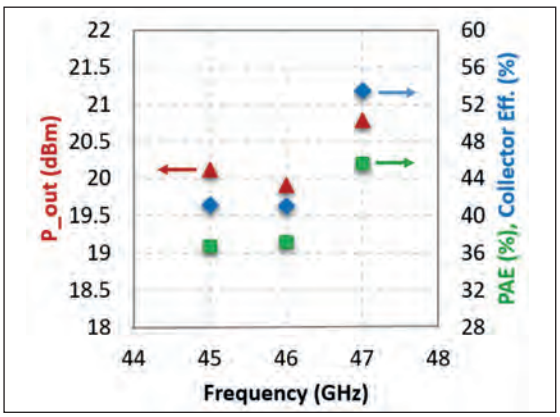

Figure 7. Summary of measured power performance at 45 GHz, 46 GHz and 47 GHz.

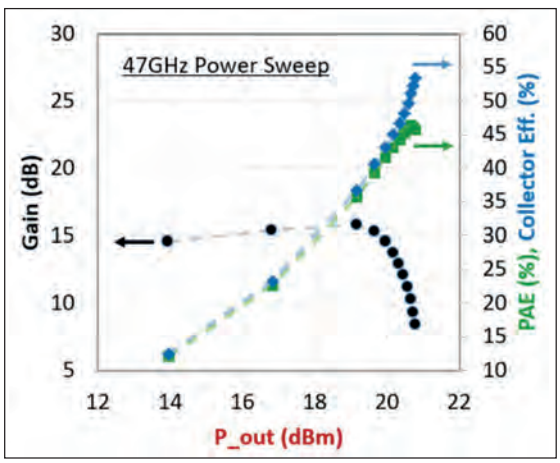

Figure 8. Measured power sweep at 47 GHz, at V_{CC}= 2.75 V and V_{BB}= 2.35 V ($I_{C,Q}$= 47 mA).

current of 32 mA that corresponds to 2.13 mA μm^{-2}, and optimum loading conditions (see Figure 4).

Based on our promising results, we selected this device, which is a common-emitter power cell with a total emitter periphery of 15 μm^2, as the key building block for producing an amplifier operating in the Q-band. We targeted an RF output power of 100 mW, for frequencies of 45 GHz to 47 GHz. For this amplifier, we decided to use a device bias point of 3.2 mA μm^{-2}, because this offers the best combination of output power and peak PAE.

At each port, we used three transmission line sections with equal impedance ratios to transform the device's optimum load and source impedance to the 50 Ω source and load. Values for load and source impedance were taken from load pull simulations at 45 GHz to 47 GHz. In this amplifier, we formed shunt capacitors by utilizing process design kit, metal-insulator-metal structures with dimensions below λ/8 at 46 GHz. Note that we did not employ thin, excessively lossy lines, because capacitance can be absorbed in intermediate line sections.

One can see our implementation of meandered microstrip lines in an optical image of our chip, shown in Figure 5. It is very compact design, with an inner area of 276 x 600 μm^2, which includes DC blocking and bypass capacitors. Including RF pads, the total area of our MMIC chip is 0.185 mm^2.

To evaluate the RF performance of our chip, we have measured the S-parameters after performing probe-tip calibration. Results are similar to what Keysight ADS simulations predict (see Figure 6). The MMIC 3 dB bandwidth is 10 GHz, giving a fractional bandwidth of roughly 20 percent.

We thinned our MMIC wafers to 76 mm to improve thermal resistance and thus heat dissipation, before undertaking power tests. Measurements at 45 GHz, 46 GHz and 47 GHz reveal a high collector efficiency, ranging from 41 percent to 53.6 percent (see Figure 7).

At 47 GHz, the frequency with the highest collector efficiency, the PAE is a record-breaking 46 percent, and the output power 119.7 mW. This is well above our 100 mW target, and if this chip were to be

Ref.	Comparison with Prior Art						
	Freq. (GHz)	Gain (dB)	P_{SAT} (dBm)	PAE (%)	Chip Area (mm^2)	Power/ A_{chip} (mW/mm^2)	Process
[1]	47	15.5	22.7	40	0.98	190	GaAs
[2]	45	10.5	20.2	31.5	1.3	80	SiGe
[3]	47	13	17.6	34.6	0.27	213	CMOS
[4]	60	10.5	23.5	43	3.05	73	InP HEMT
[5]	59	8	25.5	41	0.36	986	GaN HEMT
This Work [6]	**47**	**16**	**20.78**	**46**	**0.185**	**647**	**InP HBT**

Table 1. Comparison of the results obtained in this work to prior art. [1] G. Lv *et al*. IEEE Microw. Wirel. Compon. Lett. **28** 530 (2018). [2] K. Datta *et al*. "A 20 dBm Q-band SiGe Class-E power amplifier with 31% peak PAE," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, 2012, pp. 1-4.A. [3] Chakrabarti *et al*. "High power, high efficiency stacked mmWave Class-E-like power amplifiers in 45nm SOI CMOS," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, 2012, pp. 1-4. [4] S. M. J. Liu *et al*. "High efficiency monolithic InP HEMT V-band power amplifier," GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 21st Annual. Technical Digest 1999 (Cat. No.99CH36369), Monterey, CA, USA, 1999, pp. 145-147. [5] M. Micovic *et al*. IEEE Electron Dev. Lett. **38** 1708 (2017) [6] A. Arias-Purdue *et al*. "A 120-mW, Q-band InP HBT Power Amplifier with 46% Peak PAE," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 1291-1294

deployed in a phased-array radar, it would enable a 40 dBm effective isotropic radiated power for the 8-element array, given an antenna gain of 4 dBi, requiring 18 dBm per transmitter element. Note that at 47 GHz, the PAE reached is above 40 percent at the 1dB compression point, highlighting its high efficiency at back-off for applications where linearity is important, and thus power back-off from saturation is required.

Benchmarking the performance of our Q-band MMIC against those made with other technologies, such as CMOS, SiGe, GaAs, and GaN, highlights the capabilities of our InP devices (see Table 1).

GaN, which is widely championed as by far the best material for making great RF devices, does deliver a high power, but compared to our InP MMIC, power gain is significantly lower and PAE slightly lower. Offering similar RF power levels to our chip is the SiGe HBT, but it operates at a lower efficiency.

For the key yardstick of chip power density per unit area (mW mm^{-2}) – evaluated by dividing the saturated power by the total chip area – our work stands out amongst the various technologies, only bettered by GaN. Considering these results as a whole, it is clear that the InP MMIC, built with 0.25 μm HBT technology, has many RF attributes, making it a very strong contender for deployment in phased-array radar.

The authors acknowledge Teledyne Scientific's support through IRAD. The authors also acknowledge Teledyne's Fabrication Operations group for the MMIC fabrication.

Further reading

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Z. Griffith *et al.* "71–95 GHz (23–40% PAE) and 96–120 GHz (19–22% PAE) high efficiency 100–130 mW power amplifiers in InP HBT," 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, 2016, pp. 1-4.

M. Urteaga *et al.* "InP HBT Integrated Circuit Technology for Terahertz Frequencies," 2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, 2010, pp. 1-4.

A. Arias-Purdue *et al.* "A 120-mW, Q-band InP HBT Power Amplifier with 46% Peak PAE," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 1291-1294, doi: 10.1109/IMS30576.2020.9223945.

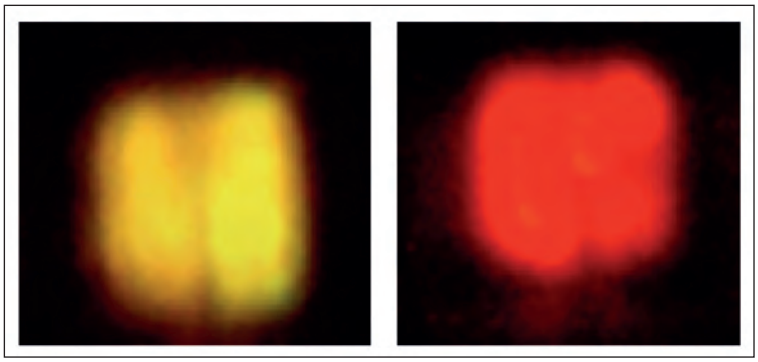
Miniaturising red microLEDs

Porosification of InGaN provides a foundation for brighter red microLEDs

RESEARCHERS at the University of California, Santa Barbara (UCSB), claim to have provided the first demonstration of InGaN-based red microLEDs with dimensions below 10 μm. Their work includes a measurement of the on-wafer external quantum efficiency (EQE) – a value of 0.2 percent.

The team's miniaturised microLED will help the development of displays based on these devices and green and blue cousins. Screens formed from a vast number of tiny LEDs promise to deliver greater contrast, higher brightness and faster response times than those produced with incumbent technologies.

Prior to the UCSB report, Soitec led the way with scaling InGaN-based red microLEDs, having reported a device with dimensions of 50 μm in 2020 and an EQE of 0.09 percent, according to an on-wafer measurement.



The team at UCSB have produced yellow and red InGaN LEDs. Images taken for a drive current of 5 A cm^{-2}.

Shubhra Pasayat, spokesperson for the UCSB team, points out that their new benchmark is an important milestone: "For viable commercialisation, microLEDs below 10 microns are extremely necessary."

Along with this small size, microLEDs need to have EQEs of at least 2-5 percent to serve in displays, argues Pasayat. Although the UCSB team is well short of that target, work is in its infancy, and substantial improvements can be expected.

The West-coast team is pursuing red microLEDs based in InGaN, rather than those made from AlGaInP and associated alloys, because the latter family suffers from a size-dependent efficiency reduction, associated with high surface recombination velocities and longer carrier diffusion lengths. In addition to this issue, which can only be partially addressed by sidewall passivation, AlGInP-based microLEDs are hampered by a higher efficiency droop with increasing temperature, due to carrier leakage over small barrier heights. To date, the best results for this class of device are dimensions of 20 μm. No figure is given for EQE.

UCSB's success hinges on the growth of devices on porous GaN pseudo-substrates. This foundation has a compliant nature, reducing strain in the indium-rich active region that delivers red emission in InGaN-based devices.

Fabrication of the microLEDs began by loading a sapphire substrate in an MOCVD chamber and depositing a 2 μm-thick unintentionally doped layer of GaN, followed by a 800 nm-thick layer of silicon-doped GaN and a 100 nm-thick unintentionally doped cap. Dry etching defined an 11 μm by 11 μm tile pattern, prior to porosification of the 800 nm-thick GaN layer.

The resulting porous GaN pseudo-substrate provided a compliant foundation for an LED structure featuring three 3 nm-thick $In_{0.26}Ga_{0.74}N$ quantum wells, each covered with a 1.5 nm-thick $Al_{0.45}Ga_{0.55}N$ cap and a 11 nm-thick GaN barrier. MicroLEDs were formed by using electron-beam evaporation to add a 110 nm-thick indium tin oxide ohmic contact on the *p*-type layer, before turning to reactive-ion etching to define 6 μm by 6 μm active regions, passivating the structure with Al_2O_3, and then adding metallic contacts.

On-wafer measurements revealed a peak at 646 nm, when driving the device at 5 A cm^{-2}. For the control – produced with the same process, but on sapphire – the peak is at 590 nm at the same current density. Pasayat and co-workers attribute the substantial difference in emission wavelength to the more efficient indium incorporation in the quantum wells grown on porous GaN pseudo-substrates.

Driven at 10 A cm^{-2}, EQE of the microLED peaks at 0.202 percent. Encapsulation should increase this figure to more than 0.6 percent. Cranking up the current to 100 A cm^{-2} propelled light output to 76 nW, corresponding to 2.1 W mm^{-2} – this output power density just exceeds that of the best AlGaInP microLEDs, which are 20 μm in size.

The team's next goal is to increase the EQE of its devices. "We are planning on improving the material quality, as well as the fabrication steps," says Pasayat.

Reference

S. Pasayat *et al*. Appl. Phys. Express **14** 011004 (2021)

GaN HEMTs deliver record efficiency

Native, treated substrates enable GaN HEMTs to surpass 80 percent power-added efficiency

ENGINEERS from Fujitsu are claiming to have raised the bar for the power-added efficiency (PAE) of GaN HEMTs operating at a few gigahertz. Their record-breaking device delivers a PAE of nearly 83 percent when operating at 2.45 GHz.

This high efficiency could help to drive down the carbon footprint of wireless infrastructure. According to findings from a project entitled *Energy Aware Radio and Network Technologies*, power amplifiers typically account for 65 percent of the energy consumption of a radio base station.

The team from Fujitsu fabricated its devices on free-standing GaN substrates, a foundation that spokesman Yusuke Kumazaki describes as "affordable". However, he admits that it's still expensive compared with other common substrates, and the price must come down to ensure commercial success of GaN-on-GaN devices.

Producing GaN HEMTs on native substrates slashes the defect density in the epilayers, leading to suppression of current collapse, a cause of degradation of power characteristics. However, prior to this latest work from Fujitsu, GaN-on-GaN HEMTs have failed to deliver the anticipated superior RF performance to siblings produced on other substrates. Kumazaki and co-workers suspected that silicon contamination at the interface was to blame for holding back the RF performance. "But the impact of silicon contamination on RF performance is much greater than our assumption," admits Kumazaki.

Note that when GaN HEMTs are grown on foreign substrates, such as silicon or SiC, silicon contamination at the growth interface is not a significant issue. That's because these epistructures feature wider bandgap materials, such as the AlN nucleation layer, where silicon does not act as a donor.

To suppress silicon impurity contamination, Fujitsu's engineers treat substrates with hydrofluoric acid before growing the epilayers. The superiority of this approach has been proven by comparing material characteristics and HEMT performance of structures produced with and without the hydrofluoric acid, wet-chemical treatment.

Devices for this study were grown by MOCVD. They featured surface passivation and a source-connected field plate, to reduce the electric field at the gate edge (see Figure 1).

Secondary-ion mass spectrometry revealed that silicon piles up at the interface between the substrate and the epilayers in GaN HEMT produced with both processes, despite the lack of intentional silicon doping. However, silicon accumulation in the control peaks at 5 x 10^{19} cm^{-3}, compared with just 8 x 10^{17} cm^{-3} in the HEMT produced with a hydrofluoric acid treatment.

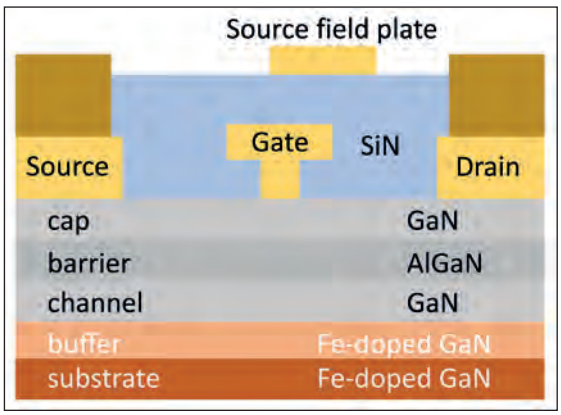


Figure 1. Fujitsu's record-breaking HEMTs are grown on native substrates.

The team investigated drain conductance and maximum stable gain, concluding that significant improvements in RF performance stem from a reduction in silicon concentration at the interface between the substrate and epilayers. RF measurements on the superior strutcure, using 10 μs pulses and a 1 percent duty cycle and a device with a 1.8 mm gate periphery, revealed a record-breaking PAE of 82.8 percent at 2.45 GHz, which is within the industrial, scientific and medical band (see Figure 2). At this frequency the output power is 42 dBm and the power density 8.7 W mm^{-1}.

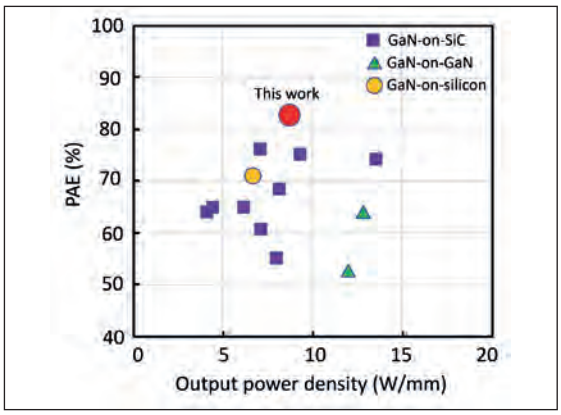


Figure 2. By preventing silicon contamination at the epilayer-substrate interface, Fujitsu's GaN HEMTs are setting a new benchmark for power-added efficiency at 2.45 GHz, which is within the industrial, scientific and medical band.

Reference

Y. Kumazaki *et al*. Appl. Phys. Express **14** 016502 (2021)

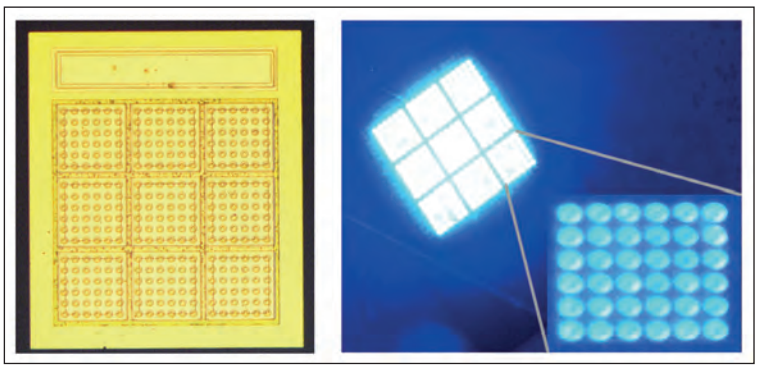
UV LEDs get smaller and brighter

Arrays of miniaturised deep-UV LEDs deliver record brightness

SCIENTISTS at the University of South Carolina are claiming to have produced the world's smallest and brightest deep-UV LEDs. Their devies, emitting at 281 nm, have dimensions down to 5 μm, with arrays producing an output of up to 361 W cm^{-2}.

The team's progress will help this class of LED compete against mercury lamps in applications requiring high doses of deep-UV radiation. For some applications, such as face-mask disinfection, the toxicity of mercury is of concern.

Led by Asif Khan, the team at the University of South Carolina pioneered interconnected arrays of tiny UV LEDs in the early years of this millennium. Introduced to combat series resistance and aid current spreading, the first generation of UV LED pixels with a 25 μm diameter provided the building blocks for 10 by 10 arrays that combined an increase in light output power with superior device reliability and reduced current crowding.



(left) Top-side micrograph of an interconnected array of 5 μm pixels with 5 μm interpixel spacing. (right) Sapphire-side micrograph of the same array under a 60 mA DC current.

Recently, the team revisited this architecture for a deep UV source, focusing this investigation on thermal impedance and the influence of pixel size on the power of the emission.

Spokesman for the latest work, Richard Floyd, told *Compound Semiconductor* that reducing the dimensions of the deep UV LEDs below 20 μm did not increase the difficulty of most fabrication steps, and did not require specialised equipment. "For instance, we used standard photoresist masking and a Karl Suss MJB-3 mask aligner for all the lithography steps."

However, to ensure good uniformity across the wafer, the team optimised the photolithography exposure/developing times for sub-20 μm features, and the *p*-ohmic contact annealing condition.

The engineers are confident that even smaller deep-UV LEDs could be produced without compromising performance. "In our study we noted that the external quantum efficiency of the interconnected micropixel arrays did not reduce with reducing pixel size," remarks Floyd. "This implies that pixel sizes smaller than those of our study may be realized without sacrificing device performance."

Note, however, that the team's results indicate that there will only be a minimal reduction in thermal impedance from further shrinking of device size.

Fabrication of the UV sources began by loading AlN-on-sapphire templates into an MOCVD chamber and depositing an epistructure that includes four 2.5 nm-thick $Al_{0.35}Ga_{0.65}N$ quantum wells and a 20 nm-thick *p*-type $Al_{0.7}Ga_{0.3}N$ electron-blocking layer. Inductively couple plasma reactive-ion etching defined pixel dimensions, before annealing under nitrogen activated the magnesium dopants and 'narrow picture frame' *n*-contacts were added, around single pixels in standalone devices and around the subarrays of pixels in interconnected devices. According to previous studies, this *n*-contact geometry precludes current crowding.

Floyd and colleagues compared the performance of a reference single-pixel LED that has a diameter of 90 μm with three different array architectures: 36 pixels with a 15 μm diameter and a 5 μm gap, 81 pixels with a 10 μm diameter and a 5 μm gap, and 324 pixels with a 5 μm diameter and a 5 μm gap.

On-wafer measurements – using 500 ns pulses and a 0.05 percent duty cycle to minimise device heating – revealed that for a single 5 μm-diameter pixel with an aluminium heat spreader, a drive current of 10.2 kA cm^{-2} led to a peak brightness of 291 W cm^{-2}. This brightness is 30 times higher than that of the reference LED.

Results from the three different arrays show that reducing the pixel size boosts performance, thanks to superior heat extraction that quashes thermal droop. Compared with the single-chip reference, the array of 324 pixels with a diameter of 5 μm delivered an increase in the output power of more than five times under CW operation, and more than 15 in pulsed mode.

The team are now exploring techniques for enhancing light extraction efficiency, and looking to leverage independent electronic control of the pixels.

Reference

R. Floyd *et al*. Appl. Phys. Express **14** 014002 (2021)

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12.04.2021

Main Event:
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(British Standard Time)

China Taiwan Time Recorded Event:
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